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Novel modular multilevel matrix converter topology for efficient high-voltage AC-AC power conversion

Introduction. *This paper delves into the practical application of multilevel technology, particularly focusing on the capacitor-clamped converter as a promising solution for medium-to-high voltage power conversion, with specific emphasis on direct AC-AC switching conditions.* ***Problem.*** *The limitations of conventional single-cell matrix converters (MC) in efficiency and performance for medium-to-high voltage power conversion applications are well-recognized.* ***Goal****. The primary objective is to investigate the performance of the 3 phase modular multilevel matrix converter (3MC) with three flying capacitors (FCs) modeling. This investigation utilizes the Venturini method for gate pulse generation, aiming to compare the performance of the 3MC with standard converter designs.* ***Methodology.*** *To achieve the research goal, the Venturini method is adopted for generating gate pulses for the 3MC, representing a departure from conventional approaches. Detailed simulations employing MATLAB/Simulink are conducted to comprehensively evaluate the performance of the 3MC in comparison to conventional converter designs.* ***Results****. The simulation outcomes reveal a significant reduction of 73 % in total harmonic distortion (THD) achieved by the 3MC. This reduction in THD indicates improved robustness and suitability for medium-to-high voltage power conversion systems necessitating direct AC-AC conversion. These results highlight the efficacy of the 3MC in enhancing power conversion efficiency and overall performance.* ***Originality****. This paper contributes novel insights into the practical implementation of multilevel technology, particularly within the realm of capacitor-clamped converters. Furthermore, the utilization of the Venturini method for gate pulse generation in the 3MC represents an original approach to enhancing converter performance.* ***Practical value.*** *The research findings present significant advancements in multilevel transformer technology, offering valuable guidance for optimizing transformer design in various industrial and renewable energy applications. These contributions serve to enhance the development of reliable and efficient power systems, addressing critical needs in the energy sector.* References 54, tables 3, figures 4.
Key words: **matrix converter, Venturini method, modular multilevel matrix converter, power conversion.**

Вступ*. У цій статті розглядається практичне застосування багаторівневої технології, зокрема, з упором на перетворювач з конденсаторною фіксацією як перспективне рішення для перетворення потужності середньої та високої напруги з особливим акцентом на умовах прямого АС-АС перемикання.* ***Проблема****. Обмеження звичайних одноелементних матричних перетворювачів (МС) в ефективності та продуктивності для додатків перетворення потужності середньої та високої напруги загальновідомі.* ***Мета****. Основною метою є дослідження продуктивності трифазного багаторівневого модульного матричного перетворювача (3МС) з моделюванням трьох навісних конденсаторів (FC). У цьому дослідженні використовується метод Вентуріні для генерації стробуючих імпульсів з метою порівняння продуктивності 3МС зі стандартними конструкціями перетворювачів.* ***Методологія****. Для досягнення мети метод Вентуріні прийнятий для генерації стробуючих імпульсів для 3МС, що є відмінністю від традиційних підходів. Проведено докладну симуляцію з використанням MATLAB/Simulink для всебічної оцінки продуктивності 3МС порівняно з традиційними конструкціями перетворювачів.* ***Результати*** *моделювання показують значне зниження на 73 % загального коефіцієнта гармонічних спотворень (THD), досягнуте 3МС. Це зниження вказує на покращену надійність та придатність для систем перетворення електроенергії середньої та високої напруги, що вимагають прямого АС-АС перетворення. Ці результати підкреслюють ефективність 3МС підвищення ефективності перетворення електроенергії та загальної продуктивності.* ***Оригінальність****. Ця стаття робить новий внесок у практичну реалізацію багаторівневої технології, особливо в області перетворювачів з конденсаторною фіксацією. Крім того, використання методу Вентуріні для генерації імпульсів затвора в 3МС є оригінальним підходом до підвищення продуктивності перетворювача.* ***Практична цінність****. Результати дослідження представляють значні досягнення в технології багаторівневих трансформаторів, пропонуючи цінні рекомендації щодо оптимізації конструкції трансформаторів у різних промислових та відновлюваних джерелах енергії. Ці вклади служать для поліпшення розробки надійних і ефективних енергосистем, задовольняючи критичні потреби в енергетичному секторі.* Бібл. 54, табл. 3, рис. 4.
Ключові слова: **матричний перетворювач, метод Вентуріні, модульний багаторівневий матричний перетворювач, перетворення потужності.**

Introduction. Matrix converters (MC) are widely used to convert AC-AC power and have wide applications in many industrial areas, advantages sinusoidal input-output current, large size reduction, and portable applications to so that eliminates large inertia. An extensive study has shown that MCs are currently considered major candidates for incorrect AC-DC-AC topologies in various industrial settings. MCs act primarily as forced switching cycle converters. Their system has a matrix of switches that can be toggled to either direction, making it easy to connect input and output wires. Regardless of MCs size and frequency, MCs offer many advantages compared to standard AC-DC-AC converters eliminating a DC link capacitor component with different specifications by directly converting AC input voltage to AC output voltage. They allow direct AC-to-AC conversion without intermediate DC phases, resulting in more straightforward configuration and improved performance. Size and weight can be significantly reduced by eliminating bulky parts such as transformers and DC link capacitors. Also, MC offer versatility in the application of different input and output voltages and frequencies, allowing them to quickly adjust to a wide variety of power source loads MCs are ideal for such rapid applications due to their high performance, fast dynamic response and improved reliability Power a precise adjustment is also important, so that fewer things can fail. In addition, they contribute to the reduction of electromagnetic interference, improvement of power quality, and decrease in harmonics, hence boosting compatibility with the grid. MCs are highly adaptable and can be used in various industrial and commercial sectors. They provide practical, flexible, and dependable solutions for power conversion.

MCs are a promising technology that is being evaluated for use in industrial applications. They are seen as a tiny AC-AC solution since they eliminate the need for

large capacitors. The fundamental theory of primarily focused on cycloconverters is presented in [1]. The Venturini method contributed significantly by suggesting a beneficial modulation for the 33 direct MCs (DMC) in [2–4]. This was done after rapidly switching pulse-width modulation (PWM) technologies, and the switches improved. Subsequently, additional versions of MCs, such as indirect MC (IMC) [5], sparse IMC [6], and ultrasparse IMC [7], were subsequently created. The study investigated the impact of impedance (*Z*) sourced, admittance (*Y*) sourced, and quasi-Z-sourced MCs on their enhancing effects [8, 9]. These topologies have also been investigated for multiphase and multilevel structures [10, 11]. Additionally, other modulation schemes, such as space vector modulation (SVM), indirect SVM, carrier-based, duty ratio-based and their modified forms have been suggested in [12–17]. Control techniques were designed to address specific difficulties, such as reducing standard mode voltage [18, 19] and optimizing commutation. The study also examined the implementation of overvoltage and overcurrent protection [20] and the inclusion of appropriate input current filters [21, 22].

Literature review. The actual advancement of MC begins with the research conducted by Venturini method, who put out a function analysis and presented the concept of a low-frequency modulation for matrix to explain the low-frequency characteristics of MC. There are two current modulation strategies for MCs that are used on carriers. One has been suggested in [23, 24], and the other was suggested in [25]. As described in [26, 27], successfully implemented indirect SVM. This modulation technique considers the 3-ph modulation constellation as a composite of a 3 phase AC-DC rectifier and a 3 phase DC inverter. Modeling the motor controller in this manner allows for utilizing the widely recognized space vector PWM for both the rectifier and inverter stages. In [28–30] the authors presented direct SVM, which relies on the instantaneous encoding of input current and output voltage using SVM. Unlike indirect SVM, the analysis encompasses all potential switching arrangements in 3 MCs and doesn't require a virtual DC link. A novel modulation technique called delta-sigma modulation, which utilizes a quantizer and a one-sample delay element, has been recently suggested for MCs [31–33]. This modulation technique is based on discrete-time or sample time. When comparing the suggested delta-sigma modulated MC to the saw-tooth and triangle carrier SVM of MC, it is observed that the proposed delta-sigma modulated converter can reduce high-frequency voltage noise peaks and preserve noise regulation [34–36].

A multilevel power converter topology is proposed to achieve high output voltage while reducing voltage stress in semiconductor switches. This enables the use of low voltage switching devices at reduced cost. In [34] the authors invented multilevel DMC by replacing the 9 bidirectional switches in a DMC with 9 H-bridges. The paper provided a comprehensive analysis of a capacitor-clamped multilevel MC, as described in [37, 38]. The voltage that was output's harmonic efficiency was clearly superior, as the findings showed. There is half the stress per switch. The increased number of switches and capacitors, which is concerning because it is twice, is what causes the harm.

Furthermore, an increase in capacitors would diminish the system's dependability. The research on mitigating standard mode voltage is conducted in reference [39]. The researchers have examined an iterative variant of multilevel DMC in [40–50]. This configuration is accomplished by incorporating numerous H-bridges in each line that link the output to the input. The advantage of such schemes is a minimal fluctuation in the output voltage, but this comes with the drawback of requiring many switches and intricate control algorithms. As a result, this topology is best suited for specialized applications. Additional research on fault detection in modular multilevel matrix converter (3MC) can be referenced in [51].

Problem definition. This type of 3MC does not belong to the category of Venturini method, as it lacks a capacitor storage element [23–27]. In [52] they have suggested using the flying capacitor (FCs) topology for the 3MC with bidirectional semiconductor switches. This topology involves the use of two FC per output phase. The charge current in the 3 output phase will experience non-uniform route impedance due to two FC per output phase and variable switching combinations. The authors in [53] have presented a 3MC with 3 FC per output phase. This solution seems effective in minimizing the impedance experienced by the charge current in the 3 output phase. While the study [54] provides a general comparison of capacitor-clamped multilevel MCs for medium-to-high voltage applications, our manuscript offers several novel contributions that distinguish it clearly. Our research specifically focuses on the practical application of a 3 phase 3MC with three FC, utilizing the Venturini method for gate pulse generation – a unique approach that allows for more precise switching control, resulting in a significant 73 % reduction in THD. Unlike the previous work [54], which uses PSCAD for simulations, we employ MATLAB / Simulink to conduct a more comprehensive analysis, providing deeper insights into converter performance under real-world operating conditions. Furthermore, our study emphasizes the practical implementation of multilevel technology in direct AC-to-AC conversion, offering detailed guidance on optimizing power conversion systems for industrial and renewable energy applications. This approach not only demonstrates superior efficiency and robustness but also provides a clear roadmap for enhancing the reliability and performance of high-voltage power systems, thereby filling critical gaps left by earlier studies.

In this study, we introduce a 3MC system featuring three FCs for each output phase, all managed by a Venturini method. This approach effectively reduces the impedance faced by the charging current while also enabling efficient triple-port control.

Goal of the article. The aims of this study are to improve the performance of 3MC to achieve 6 output voltage levels by adding 3 FC at each output stage and to reduce total harmonic distortion (THD) at both output stage and line voltage.

3MC with 3 FC per output phase. Figure 1 [53] illustrates the 3 phase AC-AC 3MC with 3 FC per output phase. IGBT switches in Fig. 1 [53] have the ability to carry current in both directions. Below is the analysis.

There are 4 switches – SAa_1, SAa_2, SBa_1, and SBa_2, together with C1. Ensure that all switches are equivalent and have the same resistance when turned off. When all 4 switches are in the off position, the voltage V_{C1} across the FC C1 (Fig. 1), may be determined using the principle of the potential divider [54]:

$$V_{C1} = (V_A - V_B)/2, \quad (1)$$

where the upper plate of V_{C1} is positively polarized, while the lower plate is negatively polarized. The same analysis applies to the other FC, C2 to C9. Therefore, $V_{C1} = V_{C4} = = V_{C7}$, $V_{C2} = V_{C5} = V_{C8}$, and $V_{C3} = V_{C6} = V_{C9}$. Applying Kirchoff's law to the switch combinations (Fig. 1) the depicted current direction corresponds to the positive half cycle of the 3 phase input voltages [54]. The IGBT bidirectional switches are configured in a shared emitter arrangement [52, 54].

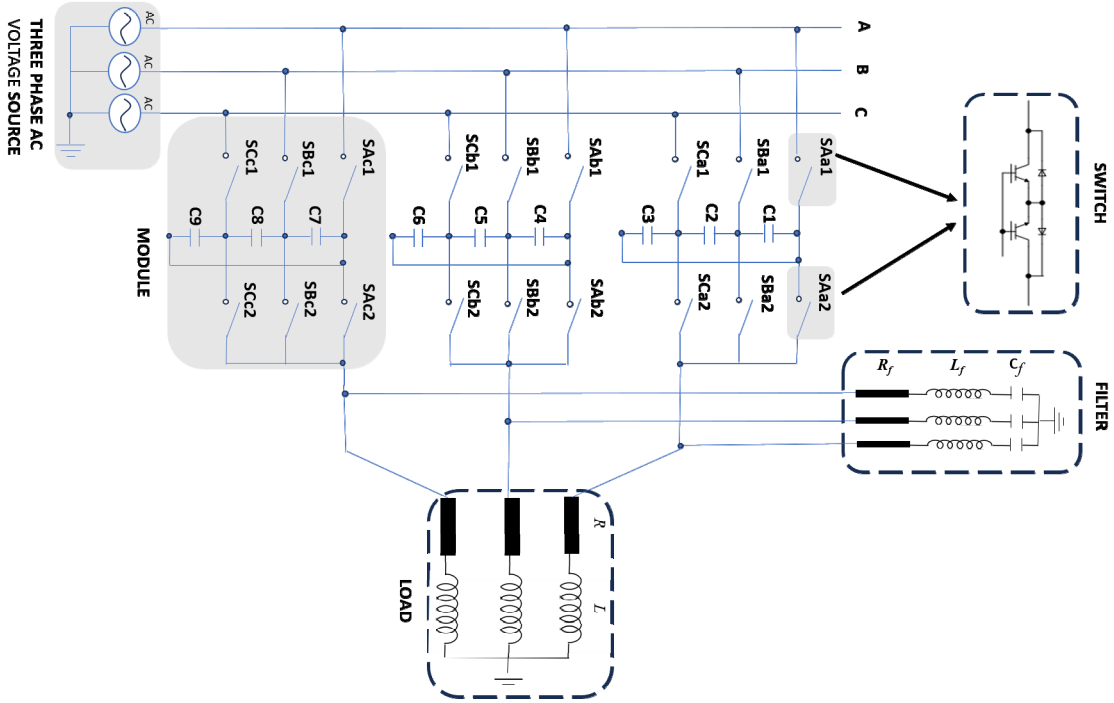

Fig1. 3 phase AC-AC 3MC with 3 FC per output phase

The capacitance C1 of the FC is determined by (2) [53]:

$$C_1 = I_0/(\Delta V_C \cdot p \cdot f_{sw}), \quad (2)$$

where I_0 is the maximum value of the load current; p is the number of cells per output phase; f_{sw} is the switching frequency; ΔV_c is the FC voltage ripple.

Control and modeling of 3MC by Venturini method. The input voltage and output voltage are determined as shown in [23–27] and presented as follows:

$$v_i = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = V_{im} \times \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + 4\pi/3) \\ \cos(\omega_i t + 2\pi/3) \end{bmatrix}; \quad (3)$$

$$v_0 = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = q \times V_{im} \times \begin{bmatrix} \cos(\omega_0 t) \\ \cos(\omega_0 t + 4\pi/3) \\ \cos(\omega_0 t + 2\pi/3) \end{bmatrix}, \quad (4)$$

where q is the voltage transfer ratio [54].

The bidirectional switches (Fig. 1) have a switching function that can be expressed as [54]:

$$S_{ijk} = \begin{cases} 1, \text{ when switch open;} \\ 0, \text{ when switch closed;} \end{cases} \quad (5)$$

$$S_{Ajk} + S_{Bjk} + S_{Cjk} = 1;$$

where $i \in$ input phase A, B, C; $j \in$ output phase a, b, c and k is the switch column counts 1, 2.

Equation (6) models the output voltage [54]. Similarly, the equation that models the input current can be expressed as (7) [54]. Equation (8) [23–27, 53] provides a straightforward approach for expressing the modulation function in terms of the unity input displacement factor.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} & S_{C1} & S_{C2} & S_{C3} \\ S_{Ab} & S_{Bb} & S_{Cb} & S_{C4} & S_{C5} & S_{C6} \\ S_{Ac} & S_{Bc} & S_{Cc} & S_{C7} & S_{C8} & S_{C9} \end{bmatrix} \times \begin{bmatrix} v_A \\ v_B \\ v_C \\ (v_A + v_B)/2 \\ (v_A + v_B)/2 \\ (v_A + v_B)/2 \end{bmatrix}, \quad (6)$$

where

$S_{Aa} = S_{Aa1} \cap S_{Aa2}$; $S_{Ba} = S_{Ba1} \cap S_{Ba2}$; $S_{Ca} = S_{Ca1} \cap S_{Ca2}$;
$S_{C1} = S_{Aa1} \cap S_{Ba2} \cup S_{Ba1} \cap S_{Aa2}$; $S_{C2} = S_{Ba1} \cap S_{Ca2} \cup S_{Ca1} \cap S_{Ba2}$;
$S_{C3} = S_{Aa1} \cap S_{Ca2} \cup S_{Ca1} \cap S_{Aa2}$;
$S_{Ab} = S_{Ab1} \cap S_{Ab2}$; $S_{Bb} = S_{Bb1} \cap S_{Bb2}$; $S_{Cb} = S_{Cb1} \cap S_{Cb2}$;
$S_{C4} = S_{Ab1} \cap S_{Bb2} \cup S_{Bb1} \cap S_{Ab2}$; $S_{C5} = S_{Bb1} \cap S_{Cb2} \cup S_{Cb1} \cap S_{Bb2}$;
$S_{C6} = S_{Ab1} \cap S_{Cb2} \cup S_{Cb1} \cap S_{Ab2}$;
$S_{Ac} = S_{Ac1} \cap S_{Ac2}$; $S_{Bc} = S_{Bc1} \cap S_{Bc2}$; $S_{Cc} = S_{Cc1} \cap S_{Cc2}$;
$S_{C7} = S_{Ac1} \cap S_{Bc2} \cup S_{Bc1} \cap S_{Ac2}$; $S_{C8} = S_{Bc1} \cap S_{Cc2} \cup S_{Cc1} \cap S_{Bc2}$;
$S_{C9} = S_{Ac1} \cap S_{Cc2} \cup S_{Cc1} \cap S_{Ac2}$;
1 = switch closed; 0 = switch open;
$\cap$= logical AND operator; $\cup$= logical OR operator;

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} (S_{Aa} \cup S_{ABa} \cup S_{ACa}) & (S_{Ab} \cup S_{ABb} \cup S_{ACb}) & (S_{Ac} \cup S_{ABc} \cup S_{ACc}) \\ (S_{Ba} \cup S_{BAa} \cup S_{BCa}) & (S_{Bb} \cup S_{BAb} \cup S_{BCb}) & (S_{Bc} \cup S_{BAc} \cup S_{BCc}) \\ (S_{Ca} \cup S_{CAa} \cup S_{CBa}) & (S_{Cb} \cup S_{CAb} \cup S_{CBb}) & (S_{Cc} \cup S_{CAc} \cup S_{CBc}) \end{bmatrix} \times \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (7)$$

where

$S_{Aa} = S_{Aa1} \cap S_{Aa2}$; $S_{ABa} = S_{Aa1} \cap S_{Ba2}$; $S_{ACa} = S_{Aa1} \cap S_{Ca2}$;
$S_{Ba} = S_{Ba1} \cap S_{Ba2}$; $S_{BAa} = S_{Ba1} \cap S_{Aa2}$; $S_{BCa} = S_{Ba1} \cap S_{Ca2}$;
$S_{Ca} = S_{Ca1} \cap S_{Ca2}$; $S_{CAa} = S_{Ca1} \cap S_{Aa2}$; $S_{CBa} = S_{Ca1} \cap S_{Ba2}$;

$S_{Ab} = S_{Ab1} \cap S_{Ab2}$; $S_{ABb} = S_{Ab1} \cap S_{Bb2}$; $S_{ACb} = S_{Ab1} \cap S_{Cb2}$;
$S_{Bb} = S_{Bb1} \cap S_{Bb2}$; $S_{BAb} = S_{Bb1} \cap S_{Ab2}$; $S_{BCb} = S_{Bb1} \cap S_{Cb2}$;
$S_{Cb} = S_{Cb1} \cap S_{Cb2}$; $S_{CAb} = S_{Cb1} \cap S_{Ab2}$; $S_{CBb} = S_{Cb1} \cap S_{Bb2}$;
$S_{Ac} = S_{Ac1} \cap S_{Ac2}$; $S_{ABc} = S_{Ac1} \cap S_{Bc2}$; $S_{ACc} = S_{Ac1} \cap S_{Cc2}$;
$S_{Bc} = S_{Bc1} \cap S_{Bc2}$; $S_{BAc} = S_{Bc1} \cap S_{Ac2}$; $S_{BCc} = S_{Bc1} \cap S_{Cc2}$;
$S_{Cc} = S_{Cc1} \cap S_{Cc2}$; $S_{CAc} = S_{Cc1} \cap S_{Ac2}$; $S_{CBc} = S_{Cc1} \cap S_{Bc2}$.

The signals that control the switches in each cell of the 3MC should be phase-shifted concerning each other by an angle of $2\pi/p$ (p is the number of switching cell, which in this example is 2). The displacement of carrier signals used to control switches S_{ij1} and S_{ij2} is $T_{sw}/2$, where $T_{sw}=1/f_{sw}$ representing the switching period. The duty cycles for the switch group are determined by comparing the modulation.

The mathematical function incorporates a saw-tooth carrier starting from its origin and compares the modulation function with a phase shifted saw-tooth carrier through a set of switches S_{ij2}, as defined by $T_{sw}/2$ [52, 53]:

$$M_{ijk} = \frac{t_{ijk}}{T_s} = \left[\frac{1}{3} + \frac{2v_i \cdot v_j}{3 \cdot V_{im}^2}\right], \quad (8)$$

for $i \in A, B, C$; and $j \in$ a, b, c and $k \in 1, 2$.

Model of output filter. The output filter circuit shown in Fig. 1 is a RLC circuit, where R_f, L_f, C_f are linked in series. The resonant frequency of this circuit is designed to be equal to the carrier switching frequency f_{sw} [54]:

$$f_{sw} = \frac{1}{2\pi\sqrt{L_f \cdot C_f}}. \quad (9)$$

Simulation results. MATLAB/Simulink model of a 3MC with 3 FC per output stage has been created. The simulation uses the settings specified in Table 1.

Table 1

3MC model parameters

Parameter	Value
Phase to ground input voltage	220 V
Input frequency	50 Hz
Output frequency	50 Hz
Modulation index q	0.5, 0.3, 0.9
Switching frequency	5 kHz
Flying capacitor	10 μF
Series RLC filter	10 Ω, 2 mH, 0.5 μF
RL load	50 Ω, 0.5 H

First test (Case 1: q = 0.5). In Fig. 2,*a* the output voltage of a 3MC with 3 FC over a period of 5 s appears to show. The output voltage appears to be a non-sinusoidal waveform, which is common for 3MC. The voltage appears to have several levels, which is characteristic of a 3MC. The voltage waveform appears to be fluctuating slightly over time. This could be due to a number of factors, such as variations in the input voltage or the load current.

Figure 2,*b* shows 3 phase load currents over a time period of 5 s. The current is ranging from –1 A to 1 A. The graph showcases 3 distinct current waveforms designated as I_a, I_b, I_c. These phases are equally spaced across the time axis, signifying a balanced 3 phase system. Each phase current adheres to a sinusoidal wave pattern, a defining characteristic of AC systems.

Figure 2,*c* shows the output voltage characteristics of a 3MC with a 3 FC for phases A, B, C. Each figure shows a comparison between input reference (black line) and output voltage (colored line). The output voltage in each figure V_a(out), V_b(out), V_c(out) show non-sinusoidal waveform with several voltage levels. This characteristic is a defining characteristic of multilevel converters. It achieves a near-sinusoidal output voltage with reduced THD compared to traditional two-level converters. The black line in each figure likely depicts the reference input voltage V_a(int), V_b(int), V_c(int). By comparing it to the output voltage, we can analyze the modulation strategy employed by the converter regulates the output voltage by manipulating the switching of its internal power electronic elements based on the reference input.

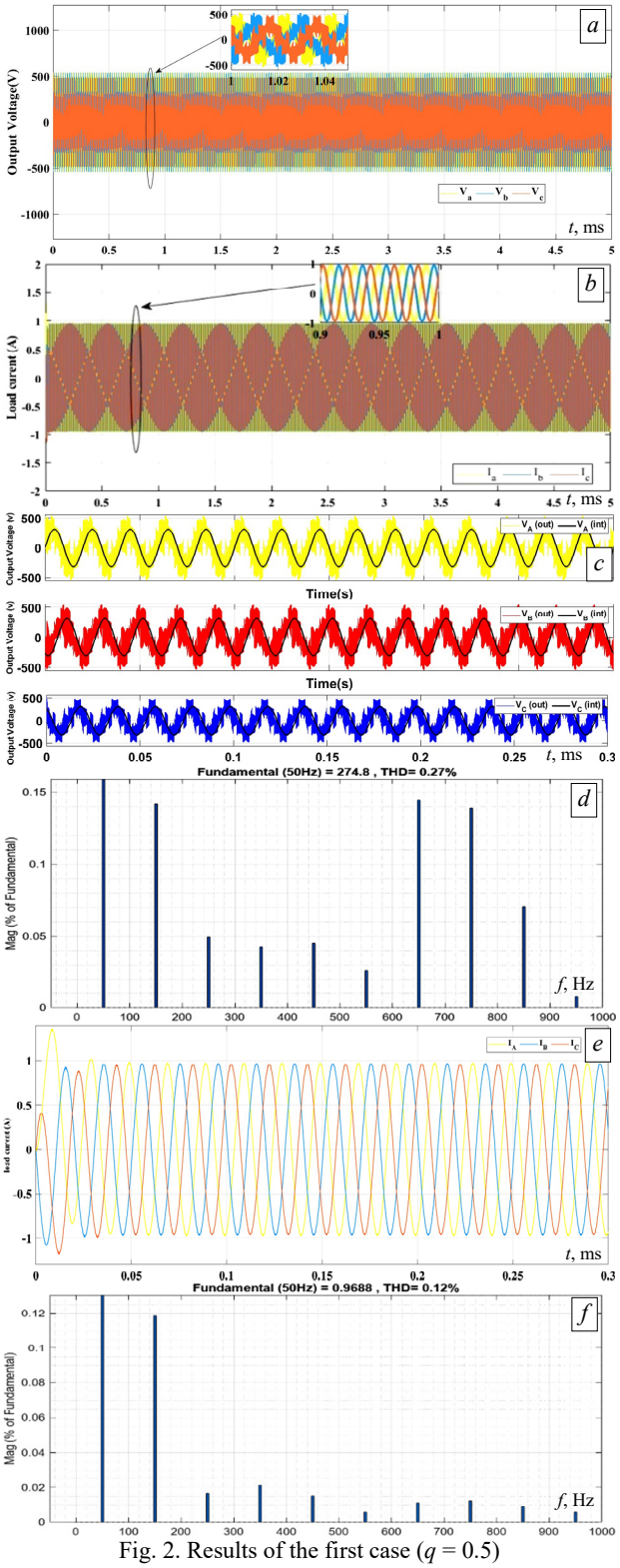

Fig. 2. Results of the first case (q = 0.5)

Figure 2,*d* shows the THD for the output voltage (phase A) with fundamental value 274.8 V and THD in this

case 0.27 % is a relatively low value. This means the voltage waveform for phase *A* is close to a pure sine wave.

Figure 2,*e* depicts 3 current waveforms, designated as «Load current» for each phase of a 3 phase system. The waveforms closely resemble sinusoids, indicating a balanced linear load with minimal harmonic distortion.

Figure 2,*f* shows the THD for the load current with fundamental value 0.9688 A and THD in this case 0.12 % is a relatively low value. This means the voltage waveform for phase *A* is close to a pure sine wave.

Second test (Case 2: q = 0.3). Figure 3,*a* depicts the output voltage behavior of a 3MC with a 3 FC across three phases *A*, *B*, and *C*. Each graph compares the reference input voltage (black line) with the output voltage for each phase (colored line). The output voltage exhibits a non-sinusoidal waveform with multiple voltage levels, a characteristic feature of multilevel converters, aiming to achieve near-sinusoidal output voltage with reduced THD compared to traditional converters. By comparing the reference input with the output voltage, the modulation strategy employed by the converter, which manipulates internal power electronic elements' switching based on the reference input to regulate the output voltage, can be analyzed.

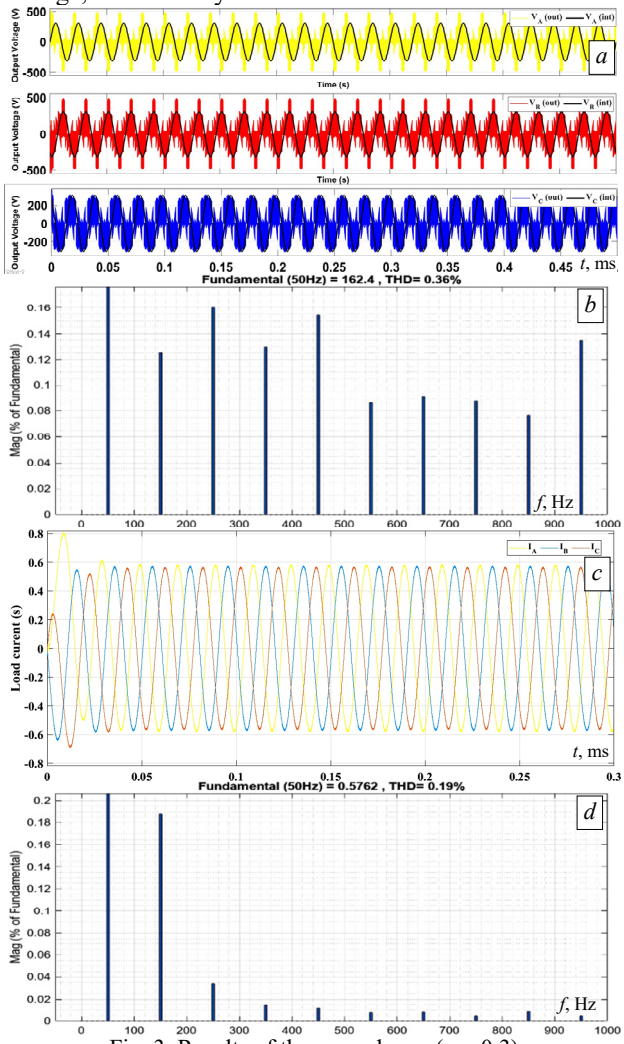

Fig. 3. Results of the second case (q = 0.3)

Figure 3,*b* depicts the THD for the output voltage (phase *A*) with value of THD in this case 0.36 % is a relatively low value. This means the voltage waveform for phase *A* is close to a pure sine wave.

Figure 3,*c* illustrates 3 current waveforms for each phase within a 3 phase system. These waveforms exhibit a close resemblance to sinusoidal patterns, suggesting a well-balanced linear load with minimal harmonic distortion. Figure 3,*d* presents the fundamental value 0.5762 A and THD value of 0.19 % is a relatively low value, indicating minimal THD in the load current. This means the current waveform is close to a pure sine wave.

Third test (Case 3: q = 0.9). Figure 4,*a* shows that the allure of the output voltage is perturbed compared to the input voltage. The top graph shows the output voltage V_A(out) and the internal voltage V_{int} plotted over time. The output voltage appears to be oscillating more frequently than the input voltage and the same comment for the middle graph and the bottom graph. In all 3 graphs, the output voltage waveform is more complex than the internal voltage waveform. This suggests that the output voltage is being perturbed by some external factor.

Figure 4,*b* depicts the THD for the output voltage (phase *A*) with fundamental value 459.2 V and THD in this case 7.31 %. Figure 4,*c* depicts 3 current waveforms for each phase. The waveforms closely resemble sinusoids, indicating a balanced linear load with harmonic distortion. Figure 4,*d* presents the fundamental value 1.719 A and THD value of 2.6 % is a relatively low value, indicating THD in the load current.

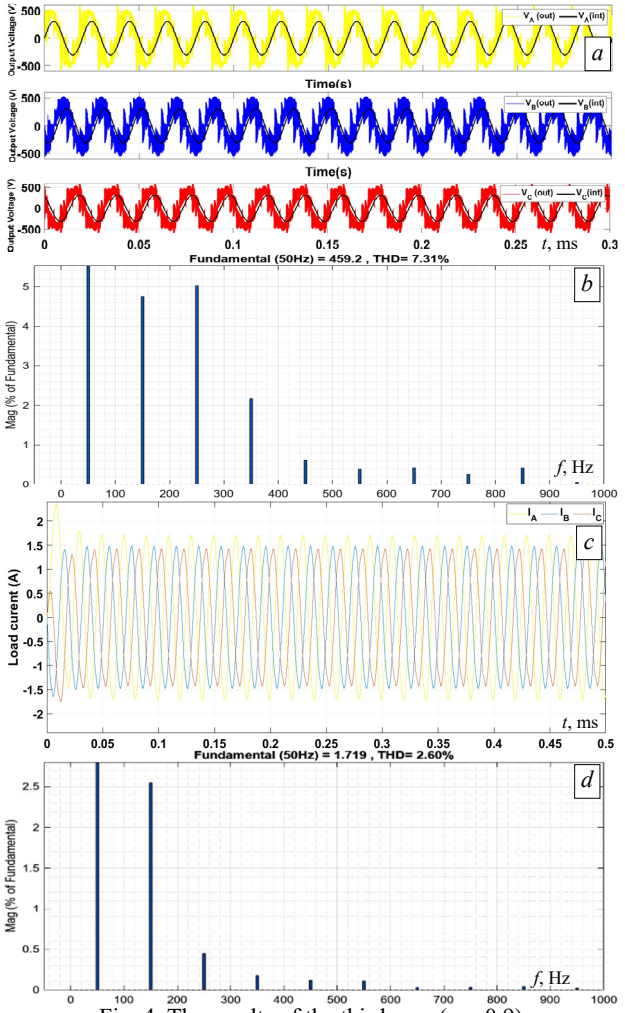

Fig. 4. The results of the third case (q = 0.9)

After analyzing Table 2, we conclude that Case 1 (q = 0.5) exhibits the best performance among the other

cases, with the lowest THD of phase *A* at 0.27 %, a peak fundamental of 274.8 V, a peak input current of 0.9688 A, and a THD of load current of 0.12 %.

Table 2

Comparison 3MC simulation results

No.	Parameters	Line to line output voltage		Phase *A* input current	
		THD, %	Peak fundamental, V	THD, %	Peak fundamental, A
Case 1	$q = 0.5$	0.27	274.8	0.12	0.9688
Case 2	$q = 0.3$	0.36	162.4	0.19	0.5762
Case 3	$q = 0.9$	7.31	459.2	2.6	1.719

Table 3 presents a comparison between the THD values of proposed 3MC and another converters. The data clearly demonstrates the significant improvement achieved by proposed 3MC in reducing THD compared to the referenced converters. Specifically, the THD reduction ratio of the 3MC, when compared with [54], is 73 %.

Table 3

A comparison between the THD values of proposed 3MC and another converters

Reference	THD of output voltage, %
Article [52]	7.78
Article [53]	23
Article [54]	1.02
Proposed 3MC	0.27

The findings from our study demonstrate notable advancements over previous works, particularly in terms of efficiency and harmonic reduction. Our research shows that the 3 phase 3MC with 3 FC, utilizing the Venturini method for gate pulse generation, achieves a 73 % reduction in THD. This significant improvement surpasses the performance metrics presented in the earlier study, where no such substantial reduction in THD was quantified. Unlike Iyer's work [54], which relied on PSCAD for simulations, our use of MATLAB/Simulink enabled a more detailed and comprehensive assessment of the 3MC's performance across various operating scenarios, allowing for a deeper understanding of its dynamic behavior, stability, and robustness. These enhanced results demonstrate the superior capability of our approach in optimizing power conversion efficiency and minimizing distortion, especially in medium-to-high voltage applications requiring direct AC-AC conversion. Moreover, our study extends the practical application of multilevel converter technology by offering concrete strategies for improving design and performance in industrial and renewable energy contexts, which were not specifically addressed in the previous work.

Conclusions. The adopted multilevel technologies, especially the capacitor-clamped matrix converter (MC), offer promising solutions for medium and high voltage power conversion needs, especially the counter-output stage introduced in this study though made a model on the modular multilevel matrix converter (3MC) of the transformer. The deviation from the conventional methods used in single-cell matrix transformers is demonstrated by the use of a Venturini method to generate gate pulses in this transformer in which using a capacitor-clamp arrangement with 3 flying capacitors.

Simulation results with using MATLAB/Simulink have shown the improved performance of the 3MC. This improvement is evident through comparisons across 3 cases and the tabulated analysis of THD in line-to-line output voltage and input current. These outcomes highlight the effectiveness of the suggested converter design in achieving enhanced performance in power conversion applications.

Recommendations and prospects for further development. To validate the simulation results, real-world implementation and testing of the 3MC under various conditions are recommended. Further optimization of Venturini method control algorithms, exploration of scalability, integration with renewable energy sources, and investigation of thermal management and long-term reliability are essential. Performing a cost-benefit analysis will offer important insights into the economic viability of this technology for industrial applications.

Conflict of interest. The authors declare that they have no conflicts of interest.

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