UDC 621.314 https://doi.org/10.20998/2074-272X.2023.6.10

E. Parimalasundar, S. Muthukaruppasamy, R. Dharmaprakash, K. Suresh

Performance investigations of five-level reduced switches count H-bridge multilevel inverter

Introduction. *This research paper describes a simple five-level single-phase pulse-width modulated inverter topology for photovoltaic grid applications. Multilevel inverters, as opposed to conventional two-level inverters, include more than two levels of voltage while using multiple power switches and lower-level DC voltage levels as input to produce high power, easier, and less modified oscillating voltage. The H-bridge multilevel inverter seems to have a relatively simple circuit design, needs minimal power switching elements, and provides higher efficiency among various types of topologies for multi-level inverters that are presently accessible. Nevertheless, using more than one DC source for more than three voltage levels and switching and conduction losses, which primarily arise in major power switches, continue to be a barrier. The* ***novelty*** *of the proposed work consists of compact modular inverter configuration to connect a photovoltaic system to the grid with fewer switches.* ***Purpose.*** *The proposed system aims to decrease the number of switches, overall harmonic distortions, and power loss. By producing distortion-free sinusoidal output voltage as the level count rises while lowering power losses, the constituted optimizes power quality without the need for passive filters.* ***Methods.*** *The proposed topology is implemented in MATLAB/Simulink with gating pulses and various pulse width modulation technique.* ***Results****. With conventional topology, total harmonic distortion, power switches, output voltage, current, power losses, and the number of DC sources are investigated.* ***Practical value.*** *The proposed topology has proven to be extremely useful for deploying photovoltaic-based stand-alone multilevel inverters in grid applications.* References 18, table 2, figures 15.

Key words: **H-bridge multilevel inverter, pulse width modulation, switching losses, total harmonic distortion.**

Вступ*. У цій дослідницькій статті описується проста топологія п'ятирівневого однофазного інвертора із широтно-імпульсною модуляцією для фотоелектричних мереж. Багаторівневі інвертори, на відміну від звичайних дворівневих інверторів, включають більше двох рівнів напруги при використанні кількох перемикачів потужності та рівнів постійної напруги нижчого рівня на вході для створення більш потужної, простішої і менш модифікованої коливальної напруги. Багаторівневий інвертор з Н-мостом, мабуть, має відносно просту схему, вимагає мінімальної кількості елементів, що перемикають, і забезпечує більш високу ефективність серед різних типів топологій багаторівневих інверторів, які доступні в даний час. Тим не менш, використання більше одного джерела постійного струму для більш ніж трьох рівнів напруги, а також втрати на перемикання та провідність, які в першу чергу виникають в основних силових перемикачах, як і раніше, залишаються перешкодою.* ***Новизна*** *запропонованої роботи полягає у компактній модульній конфігурації інвертора для підключення фотоелектричної системи до мережі з меншою кількістю перемикачів.* ***Мета****. Пропонована система спрямована на зменшення кількості перемикачів, загальних гармонічних спотворень та втрат потужності. Створюючи синусоїдальну вихідну напругу без спотворень у міру збільшення рівня та одночасно знижуючи втрати потужності, перетворювач оптимізує якість електроенергії без необхідності використання пасивних фільтрів.* ***Методи****. Запропонована топологія реалізована в MATLAB/Simulink з використанням стробуючих імпульсів та різних методів широтно-імпульсної модуляції.* ***Результати****. За традиційної топології досліджуються загальні гармонічні спотворення, силові ключі, вихідна напруга, струм, втрати потужності та кількість джерел постійного струму.* ***Практична цінність****. Запропонована топологія виявилася надзвичайно корисною для розгортання автономних багаторівневих інверторів на фотоелектричній основі у мережних додатках.* Бібл. 18, табл. 2, рис. 15.

Ключові слова: **багаторівневий інвертор Н-мосту, широтно-імпульсна модуляція, комутаційні втрати, загальні гармонічні спотворення.**

1. Introduction. Multilevel inverters (MLIs) have become widely used as power converters for DC-AC power conversion in medium and high voltage/power applications, including those involving renewable energy sources, motor drives, and power systems like flexible AC transmission system and high voltage DC transmission systems. The MLI has gained acceptance as a result of its many benefits. These benefits include wider effects voltage, lower output voltage harmonic distortion, less voltage stress on the switches, low voltage ratings for high voltage applications, and smaller filters, to name a few. Most residential or low-power applications with power ranges under 10 kW use single-phase grid-connected inverters [1]. Numerous single-phase grid-connected inverter types have been the subject of studies [2].

Conventional MLI topologies include the cascaded H-bridge (CHB), flying capacitor (FC), and diode-clamped. However, these topologies have a greater number of components and more levels of capacitor voltage balancing. There have, however, been a number of MLI topologies with fewer switches proposed [3, 4]. The majority of renewable energy sources have had low output voltages. The boosting has traditionally been a crucial component of topologies used in higher voltage applications. The capacitor voltage disparity flaw affects both neutral point clamped (NPC) and FC configurations. As a result, balancing the voltages of capacitors requires the use of an auxiliary stability circuit, a sophisticated control algorithm, current/voltage sensors, and a recognition circuit. When their output reaches the desired level and a rapid increase in the number of power switches, power diodes, and capacitors used, the cost and regulate difficulty will be very high. In comparison to FC and NPC topologies, the conventional CHB topology can produce a significant output level with module cascading, and the voltage balance of the capacitor can be avoided because multiple symmetric/asymmetric DC sources are synthesized and used in the multilevel output. Finding enough unbiased sources is a major issue for the majority of practical uses [5, 6].

Single-phase MLIs can play an important role in this area, converting the photovoltaic (PV) system's DC voltage into a continuous AC signal accessible by loads as well as the gird significantly fewer harmonic filters and increased performance. The seven-level power conditioning unit inverter has been proposed for this purpose, with appealing features such as low number of switches and the ability to generate multiple voltage ranges at the result [7, 8].

Recently, it has been shown that five-level switched capacitor-based inverters are capable of producing higher voltage progress [9-12]. In [13] authors give an example based on an extendable switched capacitor module. Compared to inverters from [14, 15], all of which do not use diodes, it induces low voltages on its switches. Use of the diodes [16-18] can reduce the number of switches. The previous discussions suggest that there is a trade-off with switched capacitor-based boost MLIs. To put it another way, using low-voltage switches typically requires using more switches and the gate-driver circuits that go with them, whereas having a high switch count requires the use of high-voltage switches. These MLIs require a greater number of switches, DC sources, diodes, and capacitors as the number of output levels rises. Increased control complexity, system size, and installation space are the results of this. Consequently, the cost of the entire system rises.

The previous drawbacks are addressed by implementing modified MLI designs based on fewer circuit elements. The following noteworthy advantages of the topology are not in any specified sequence: The output voltage amplitude in the suggested topology can rise by as much as 4 times the magnitude of the DC source voltage. Designing switching patterns for power electronic switches involves the widely used multicarrier pulse width modulation (PWM) technique. Investigations have been made into the effects of variable loads on the current and voltage total harmonic distortion (THD) values. The five-level inverter has a significantly lower component count when compared to other inverters. Adding a suitable RL load have been assist in reducing the circuit's output voltage ripple.

Depending on the output voltage level, different common MLI configurations require different amounts of components. This suggests that the quantity of components will increase along with the output voltage levels. The main structural components of the multilevel converters are switches and related gate drive circuits. Size, cost, and control complexity of the inverter circuit all increase as the number of components does. In Fig. 1 a MLI with a PV application is illustrated. The proposed topology of five-level inverters and five power semiconductor switches is shown in Fig. 2.

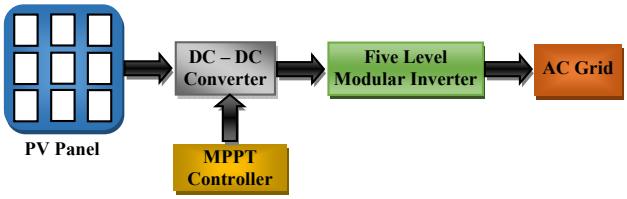

Fig. 1. PV fed proposed five-level MLI to AC grid integration

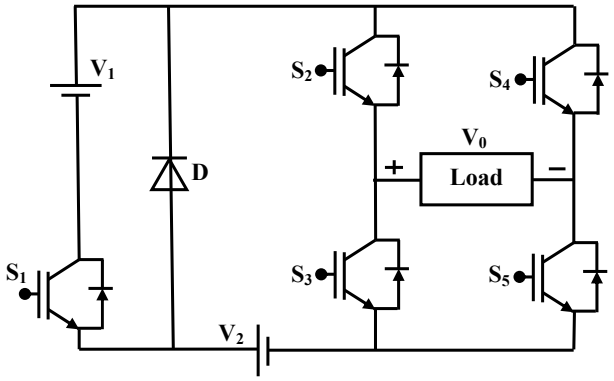

Fig. 2. Proposed topology of five-level MLI

2. Proposed topology and modes of operation. Power semiconductors are used in a MLI to create a staircase waveform from various DC levels. The 8 IGBT switches on the five-level output voltages of conventional MLI have been designed. The newly proposed topology with a reduced switch count of 5 IGBT switches is further discussed in this article. Figure 3 depicts the switching process of the proposed MLI, which results in a $+2V_{dc}$ output voltage. Similar to $+V_{dc}$, $0V_{dc}$, $-V_{dc}$, and $-2V_{dc}$ output voltages, which are depicted in Fig. 4-7 respectively, switching patterns of MLI are used to determine these voltages. Figure 8 illustrates the sinusoidal PWM used to generate switching patterns based on a signal with one reference wave and 4 carriers.

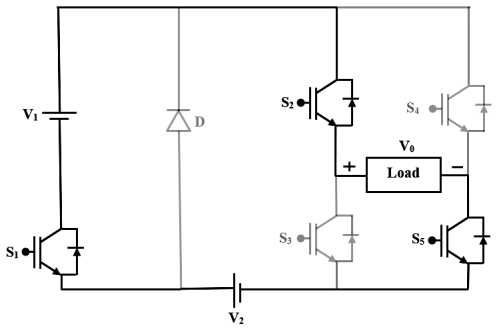

Fig. 3. Mode-I operation

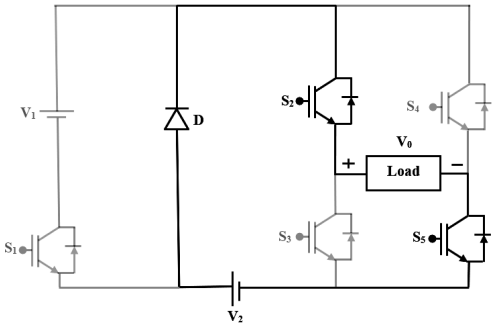

Fig. 4. Mode-II operation

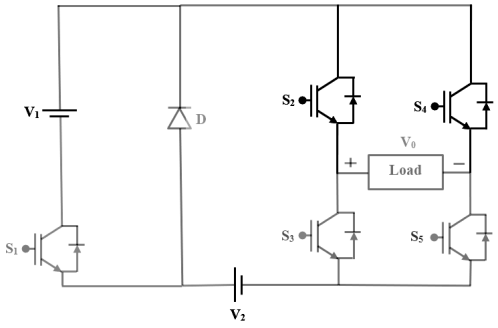

Fig. 5. Mode-III operation

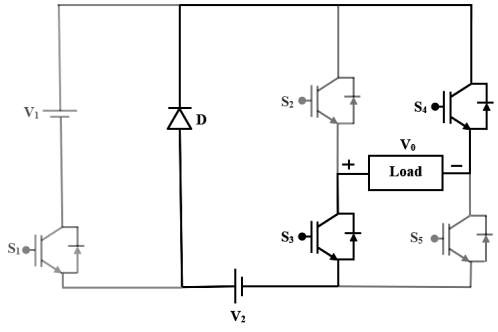

Fig. 6. Mode-IV operation

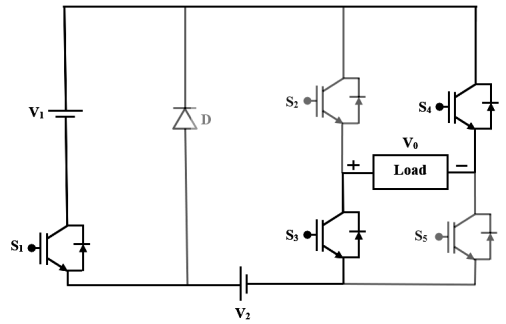

Fig. 7. Mode-V operation

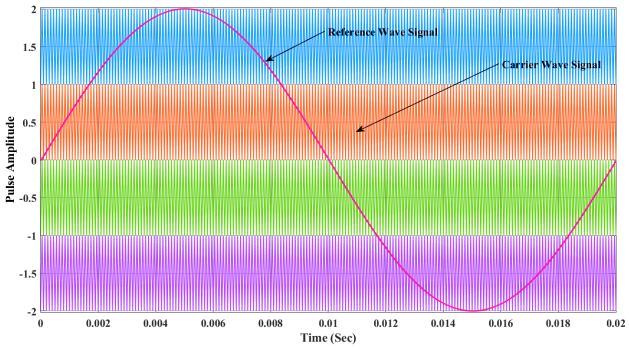

Fig. 8. Sinusoidal PWM for generating switching patterns

3. Results and discussion. Figure 9 shows the output voltage and current of the suggested MLI for a resistive load, which provides a 220V staircase five-level output voltage and current patterns which complement the output voltage patterns of resistive load. The output voltage and current of the proposed MLI for a resistive load are shown in Figure 10, which produces a 220V staircase output voltage but almost sinusoidal current patterns owing to the inductive load. Figure 11 has shown a THD analysis of the proposed MLI's output voltage under a resistive load. The output current of the proposed MLI under a resistive load is shown in THD analysis in Fig. 12. Figure 13 has shown a THD analysis of the proposed MLI's output current under a resistive and inductive load.

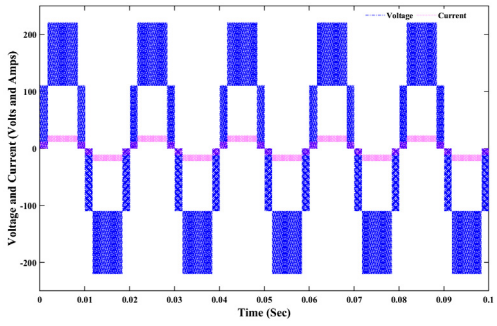

Fig. 9. Output voltage and current of proposed MLI for resistive load

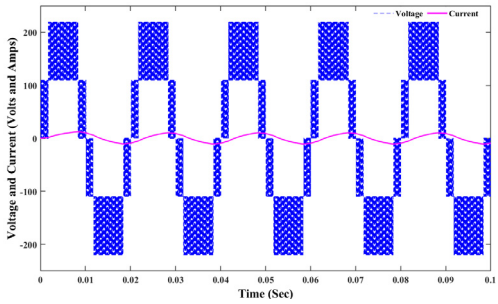

Fig. 10. Output voltage and current of proposed MLI for RL load

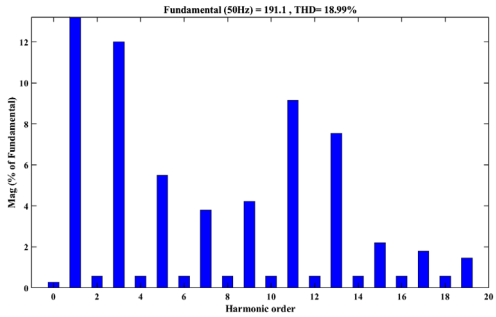

Fig. 11. THD analysis of output voltage of proposed MLI during R load

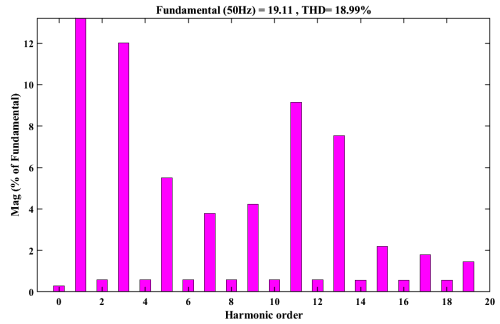

Fig. 12. THD analysis of output current of proposed MLI during R load

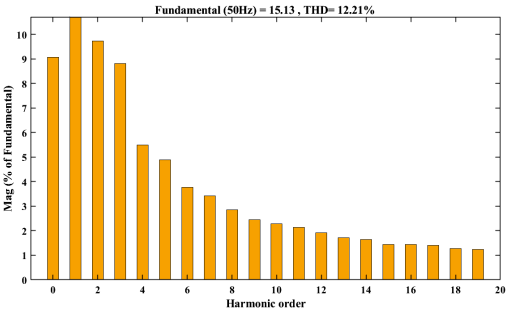

Fig. 13. THD analysis of output current of proposed MLI during RL load

4. Power loss and comparative analysis. The losses in the developed proposed structure are mostly intense on 3 main power losses, specifically losses during switching ($W_{Switching}$) and conduction ($W_{conduction}$). Then overall power loss (W_{Loss}) of MLI is written as:

$$W_{Loss} = W_{Switching} + W_{Conduction} \cdot \quad (1)$$

Conduction loss of power semiconductor devices is calculated as:

$$W_{Conduction} = \int_0^{T_0/2} \left\{ \begin{array}{l} \left[V_{CE0} + r i_p \sin(\omega t)\right] \times \\ \times i_p \sin(\omega t) \left[\frac{1}{2}\left(1 + A_m \sin(\omega t + \varphi)\right)\right] \end{array} \right\} \mathrm{d}t,$$

after simplification of above equation:

$$W_{Conduction} = \frac{1}{2} \left\{ \begin{array}{l} \left(V_{CEO} \cdot \frac{i_p}{\pi} + r \cdot \frac{i_p^2}{4} \right) + \\ + \left(A_m \cdot \cos\varphi \cdot V_{CEO} \cdot \frac{i_p}{8} \right) + \left(\frac{1}{3\pi} \cdot r i_p^2 \right) \end{array} \right\}, \quad (2)$$

where V_{CEO} is the zero-current collector to emitter voltage; r is the collector to emitter on-state resistance; A_m is the modulation index; i_p is the peak current of IGBT device.

Switching loss is expressed as the integration of all the turn-on and turn-off switching energies at the switching instants. In the equation, variable switching time is considered and integrated as:

$$W_{Switching} = f_{sw} \frac{1}{T_0} \int_0^{T_0/2} \left(E_{on} + E_{off}\right) \cdot \left(t, i_p\right) \mathrm{d}t \,, \qquad (3)$$

where T_0 is the switching time period; f_{sw} is the switching frequency; E_{on} is the on-state voltage drop; E_{off} is the off-state voltage drop.

The efficiency of MLI is calculation as:

$$Efficiency = \frac{P_{Output}}{P_{Output} + W_{Loss}} \cdot 100\% \,. \qquad (4)$$

Table 1 shows the results of various power loss and efficiency calculations based on mathematical expressions.

Table 1

THD, power loss and conduction loss parameters of proposed five-level MLI

Parameters	Conventional H-bridged topology	Proposed H-bridged topology
No. input DC supply (symmetrical)	2	2
DC voltage (magnitude), V	110	110
RMS output voltage, V	220	220
No. of IGBTs	8	5
No. gating circuits	8	5
Carrier frequency, kHz	2	2
THD current (RL load), %	18.99	12.21
$W_{switching\ loss}$, W	0.32	0.24
$W_{conduction\ loss}$, W	48.25	45.31
W_{Loss}, W	48.81	45.55
Efficiency, %	91.63	95.52

Table 2 depicts the fundamental parameters of conventional and proposed MLI.

Table 2

Parameters of conventional and proposed MLI

Parameters	DC	FC	CHB	Proposed MLI
DC supply	1	1	2	2
Switches	8	8	8	5
Diodes	12	–	–	1
DC bus capacitors	4	4	–	–
Balancing capacitors	0	6	–	–

Figure 14 has shown a THD analysis of the output current of the proposed MLI under a resistive load, and Figure 15 illustrates an efficiency comparison between the proposed and conventional MLI.

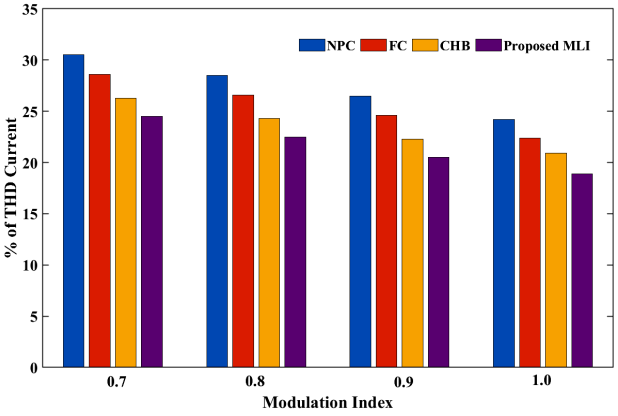

Fig. 14. THD analysis of output current of proposed MLI during resistive load

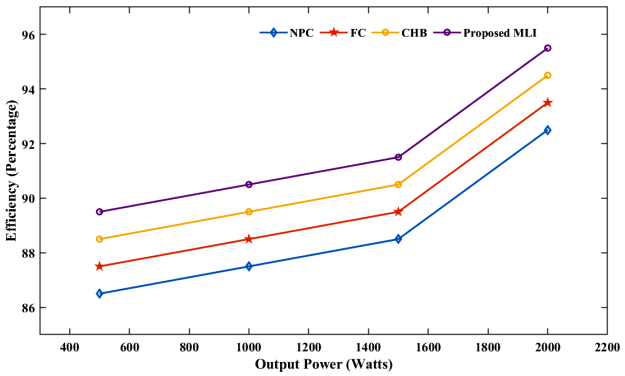

Fig. 15. Efficiency analysis of conventional and proposed MLI

5. Conclusions. It is observed that a five-level converter that is able to reconfigure and makes use of fewer power switches satisfies multilevel inverter requirements. The used five-level inverter produced 5 levels of RMS output staircase voltage when the power switches were given the proper pulse width modulation signal in a logical manner. Using the MATLAB/Simulink, total harmonic distortion values between 12.21 % distances with various loads were obtained and examined. The proposed converter is 95.52 % efficient when input, output, and power losses are taken into account. Comparisons show that the suggested single-phase five-level inverter performs significantly better than traditional converters.

Conflict of interest. The authors declare that they have no conflicts of interest.

REFERENCES

1. Odeh C., Lewicki A., Morawiec M., Kondratenko D. Three-Level F-Type Inverter. *IEEE Transactions on Power Electronics*, 2021, vol. 36, no. 10, pp. 11265-11275. doi: https://doi.org/10.1109/TPEL.2021.3071359.

2. Parimalasundar E., Kumar N.M.G., Geetha P., Suresh K. Performance investigation of modular multilevel inverter topologies for photovoltaic applications with minimal switches. *Electrical Engineering & Electromechanics*, 2022, no. 6, pp. 28-34. doi: https://doi.org/10.20998/2074-272X.2022.6.05.

3. Parimalasundar E., Senthil Kumar R., Chandrika V.S., Suresh K. Fault diagnosis in a five-level multilevel inverter using an artificial neural network approach. *Electrical Engineering & Electromechanics*, 2023, no. 1, pp. 31-39. doi: https://doi.org/10.20998/2074-272X.2023.1.05.

4. Sonti V., Jain S., Bhattacharya S. Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter. *IEEE Transactions on Power Electronics*, 2017, vol. 32, no. 2, pp. 1156-1169. doi: https://doi.org/10.1109/TPEL.2016.2550206.

5. Suresh K., Parimalasundar E. IPWM Based IBMSC DC-AC Converter Using Solar Power for Wide Voltage Conversion System. *IEEE Canadian Journal of Electrical and Computer Engineering*, 2022, vol. 45, no. 4, pp. 394-400. doi: https://doi.org/10.1109/ICJECE.2022.3207873.

6. Meneses D., Blaabjerg F., Garcia O., Cobos J.A. Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application. *IEEE Transactions on Power Electronics*, 2013, vol. 28, no. 6, pp. 2649-2663. doi: https://doi.org/10.1109/TPEL.2012.2227820.

7. Mhiesan H., Wei Y., Siwakoti Y.P., Mantooth H.A. A Fault-Tolerant Hybrid Cascaded H-Bridge Multilevel Inverter. *IEEE Transactions on Power Electronics*, 2020, vol. 35, no. 12, pp. 12702-12715. doi: https://doi.org/10.1109/TPEL.2020.2996097.

8. Jahan H.K., Panahandeh F., Abapour M., Tohidi S. Reconfigurable Multilevel Inverter with Fault-Tolerant Ability.

IEEE Transactions on Power Electronics, 2018, vol. 33, no. 9, pp. 7880-7893. doi: https://doi.org/10.1109/TPEL.2017.2773611.

9. Suresh K., Parimalasundar E. Design and Implementation of Universal Converter. *IEEE Canadian Journal of Electrical and Computer Engineering*, 2022, vol. 45, no. 3, pp. 272-278. doi: https://doi.org/10.1109/ICJECE.2022.3166240.

10. Siddique M.D., Mekhilef S., Rawa M., Wahyudie A., Chokaev B., Salamov I. Extended Multilevel Inverter Topology with Reduced Switch Count and Voltage Stress. *IEEE Access*, 2020, vol. 8, pp. 201835-201846. doi: https://doi.org/10.1109/ACCESS.2020.3026616.

11. Saeedian M., Adabi M.E., Hosseini S.M., Adabi J., Pouresmaeil E. A Novel Step-Up Single Source Multilevel Inverter: Topology, Operating Principle, and Modulation. *IEEE Transactions on Power Electronics*, 2019, vol. 34, no. 4, pp. 3269-3282. doi: https://doi.org/10.1109/TPEL.2018.2848359.

12. Suresh K., Parimalasundar E., Jayakumar S., Ravikumar R. Encapsulated 3Ø converter for power loss minimization in a grid-connected system. *Automatika*, 2023, vol. 64, no. 1, pp. 189-197. doi: https://doi.org/10.1080/00051144.2022.2119501.

13. Sandeep N., Yaragatti U.R. Design and Implementation of a Sensorless Multilevel Inverter with Reduced Part Count. *IEEE Transactions on Power Electronics*, 2017, vol. 32, no. 9, pp. 6677-6683. doi: https://doi.org/10.1109/TPEL.2017.2681739.

14. Parimalasundar E., Jayakumar S., Ravikumar R., Suresh K. Investigation analysis of open circuit and short circuit fault on cascaded H-bridged multilevel inverter using artificial neural network approach. *International Journal of Electrical and Electronics Research*, 2022, vol. 10, no. 2, pp. 320-326. doi: https://doi.org/10.37391/ijeer.100243.

15. Maalandish M., Hosseini S.H., Jalilzadeh T. High step-up dc/dc converter using switch-capacitor techniques and lower losses for renewable energy applications. *IET Power Electronics*, 2018, vol. 11, no. 10, pp. 1718-1729. doi: https://doi.org/10.1049/iet-pel.2017.0752.

16. Parimalasundar E., Suresh K., Sindhuja R., Manikandan K. A Performance Investigations of Modular Multilevel Inverter with Reduced Switch Count. *2022 International Conference on Intelligent Innovations in Engineering and Technology (ICIIET)*, 2022, pp. 83-87. doi: https://doi.org/10.1109/ICIIET55458.2022.9967595.

17. Belbachir N., Zellagui M., Settoul S., El-Bayeh C.Z., Bekkouche B. Simultaneous optimal integration of photovoltaic distributed generation and battery energy storage system in active distribution network using chaotic grey wolf optimization. *Electrical Engineering & Electromechanics*, 2021, no. 3, pp. 52-61. doi: https://doi.org/10.20998/2074-272X.2021.3.09.

18. Parimalasundar E., Jayanthi R., Suresh K., Sindhuja R. Investigation of efficient multilevel inverter for photovoltaic energy system and electric vehicle applications. *Electrical Engineering & Electromechanics*, 2023, no. 4, pp. 47-51. doi: https://doi.org/10.20998/2074-272X.2023.4.07.

Received 30.01.2023
Accepted 27.04.2023
Published 02.11.2023

Ezhilvannan Parimalasundar[1], *Professor,*
S. Muthukaruppasamy [2], *Professor,*
R. Dharmaprakash[3], *Professor,*
Krishnan Suresh[4], *Associate Professor,*
[1] Department of Electrical & Electronics Engineering,
Mohan Babu University (Erstwhile Sree Vidyanikethan Engineering College), Tirupati, AP – 517102, India,
e-mail: parimalasundar.e@vidyanikethan.edu (Corresponding Author)
[2] Electrical and Electronics Engineering,
Velammal Institute of Technology,
Anna University, Panchetti, TN – 601204, India,
e-mail: mksamy14@yahoo.com
[3] Department of Electrical and Electronics Engineering,
Panimalar Engineering College, Chennai – 600123, India,
e-mail: rdharmaprakash@yahoo.co.in
[4] Department of Electrical and Electronics Engineering,
Christ (Deemed to be University), Bangalore, India,
e-mail: sureshk340@gmail.com

How to cite this article:
Parimalasundar E., Muthukaruppasamy S., Dharmaprakash R., Suresh K. Performance investigations of 5-level reduced switches count H-bridge multilevel inverter. *Electrical Engineering & Electromechanics*, 2023, no. 6, pp. 58-62. doi: https://doi.org/10.20998/2074-272X.2023.6.10