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Integrated through-silicon-via-based inductor design in buck converter for improved efficiency

*Introduction. Through-silicon-via (TSV) is one of the most important components of 3D integrated circuits. Similar to two-dimensional circuits, the performance evaluation of 3D circuits depends on both the quality factor and inductance. Therefore, accurate TSV-inductor modeling is required for the design and analysis of 3D integrated circuits. **Aim.** This work proposes the equivalent circuit model of the TSV-inductor to derive the relations that determine both the quality factor and the inductance by Y-parameters. **Methods.** The model developed was simulated using MATLAB software, and it was used to evaluate the effect of redistribution lines width, TSV radius, and the number of turns on inductance and quality factor. Additionally, a comparative study was presented between TSV-based inductors and conventional inductors (i.e., spiral and racetrack inductors). **Results.** These studies show that replacing conventional inductors with TSV-inductors improved the quality factor by 64 % compared to a spiral inductor and 60 % compared to a racetrack inductor. Furthermore, the area of the TSV-inductor was reduced up to 1.2 mm². Using a PSIM simulator, the application of an integrated TSV-inductor in a buck converter was studied, and the simulation gave very good results in 3D integration compared to 2D integration. Moreover, the simulation results demonstrated that using a TSV-inductor in a buck converter could increase its efficiency by up to 15 % and 6 % compared to spiral and racetrack inductors, respectively.* References 21, tables 3, figures 8.*
Key words: **through-silicon-via-based inductor, 3D integration, buck converter, efficiency.**

*Вступ. Наскрізне з'єднання кремнію (TSV) є одним з найважливіших компонентів тривимірних інтегральних схем. Подібно до двовимірних схем, оцінка продуктивності тривимірних схем залежить як від добротності, так і від індуктивності. Тому для проєктування та аналізу тривимірних інтегральних схем необхідне точне моделювання TSV-індуктора. **Мета.** У цій роботі пропонується еквівалентна модель схеми TSV-індуктора для виведення співвідношень, що визначають як добротність, так і індуктивність за Y-параметрами. **Методи.** Розроблена модель була змодельована з використанням програмного забезпечення MATLAB та використана для оцінки впливу ширини ліній перерозподілу, радіусу TSV та кількості витків на індуктивність та добротність. Крім того, було представлено порівняльне дослідження між індукторами на основі TSV та звичайними індукторами (тобто спіральними та індукторами типу бігова доріжка). **Результати.** Ці дослідження показують, що заміна звичайних індукторів на TSV-індуктори покращила добротність на 64 % порівняно зі спіральним індуктором і на 60 % порівняно з індуктором типу бігова доріжка. Крім того, площа TSV-індуктора була зменшена до 1,2 мм². За допомогою симулятора PSIM було вивчено застосування вбудованого дроселя TSV в знижувальному перетворювачі, і моделювання дало дуже хороші результати при 3D-інтеграції порівняно з 2D-інтеграцією. Більш того, результати моделювання показали, що використання TSV-індуктора в понижувальному перетворювачі дозволяє підвищити його ефективність до 15% та 6 % порівняно зі спіральними індукторами та індукторами типу бігова доріжка відповідно. Бібл. 21, табл. 3, рис. 8.*
Ключові слова: **індуктор на основі кремнію, 3D-інтеграція, знижуючий перетворювач, ефективність.**

Introduction. In recent years, technological advancements have enabled several functions to be combined into one chip by increasing passive components while maintaining the same chip area [1-3]. However, the scaling process in 2D technology has the effect of wasting energy for the integrated passive components, resulting in an inefficient system [4]. It is possible to resolve this latter issue using 3D integration due to its superior performance in comparison to 2D [5, 6]. 3D integration is a new technical approach to scientific progress that distinguishes itself from its 2D counterpart by its high efficiency, smaller area, and lower cost [7]. Several technologies including 3D integration exist, with the most important being integrated circuits based on through-silicon-via (TSV). As a solution to the aforementioned problems associated with planar inductors, a TSV-inductor is suggested in a buck converter [8]. The structure of TSV-based inductors is the most compact in design with fewer parasites and is used in a wide variety of applications [9].

To address the problems encountered with 2D inductors, several studies have been conducted in the literature to exploit TSVs. These studies include Zhang et al. (2010) [10], Bontzios et al. (2011) [11], and Feng et al. (2012) [12]. In 2013, Tida et al [13] attempted to employ TSVs in vertical inductors for radio frequency applications.

The main contributions of this article are as follows: we are the first to study the behavior of TSV-inductors at high frequencies. Additionally, we compare the effects of 3D inductors with 2D inductors on the efficiency of the buck micro-converter.

This work is organized as follows: first, a theoretical study of the TSV-inductor is presented, highlighting its equivalent electrical circuit. Second, simulation results are presented, showing the influence of the geometric parameters of the 3D inductor. Finally, this paper concludes by demonstrating how the efficiency of the buck converter can be improved using the proposed TSV-inductor and comparing it with two other inductors.

Design and modeling TSV-inductor. There is a strong relationship between the performance of the TSV-inductor and its geometric parameters.

Figure 1 shows the typical structure of a TSV-based 3D inductor, which consists of three basic parts: the TSV, which is cylindrical in shape, and the upper and lower redistribution lines (RDLs) that's have rectangular forms.
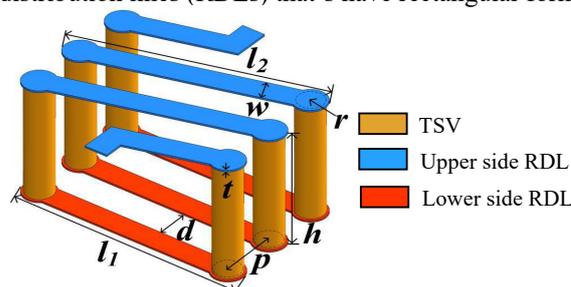

Fig. 1. Typical structure of TSV-inductor

The variables defining the geometry are the height h and radius r of the TSV, the length l, the width w, and the thickness t of each conductor, and the spacing d and the number of turns N. Copper is used as the metal material for these elements, and SiO_2 is used as the insulating material between the substrate and the copper lines.

Table 1 summarizes all geometric parameters that are essential factors in the performance of the TSV-inductor.

Table 1
Geometrical parameters of TSV-inductor

Parameter	Value
TSV height h, μm	80
TSV radius r, μm	12
Number of turns N	3
RDL length l, μm	150
RDL width w, μm	20
RDL thickness t, μm	6
Spacing between RDLs d, μm	15

The structure has two positive features: it greatly reduces the inductor printing space (lowering costs), and the design is greatly simplified. There are many equivalent circuit models for on-chip spiral inductors, but these models are rarely applied to inductors with TSVs.

As shown in Fig. 2,*a*, a π-equivalent circuit model has been developed for the higher frequency ranges [14]. The parameters of this model are: the capacitance between the redistribution lines adjacent C, the inductance series of the redistribution lines L_s, the resistance series of the redistribution lines R_s, the capacitance between the TSV and the substrate C_{ox}, the capacitance of the substrate C_{sub} and the resistance of the substrate R_{sub}, which represent the resistance, inductance, and capacitance characteristics of RDL and TSV [15, 16]. As shown in Fig. 2,*b*, these parameters of the circuit model can be derived from the Y-parameters: elements of admittance series Y_a and the elements of admittance shunt Y_b, and Y_c [17].
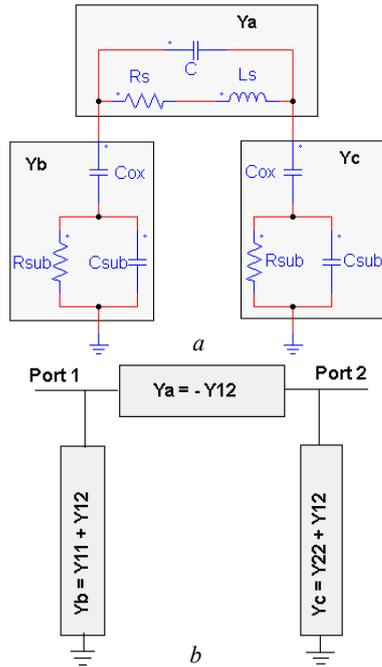

Fig. 2. *a* – equivalent circuit model of TSV-inductor;
b – π-model of two-port network

The definition of TSV-inductors is mainly based on two parameters; quality factor Q and inductance L. These latter are given by the Y parameters through the following equations [18, 19]:

$$L = \frac{\mathrm{Im}(1/Y_{11})}{\omega}, \quad (1)$$

where $\omega = 2\pi f$ and f is the frequency,

$$Q = \frac{\mathrm{Im}(1/Y_{11})}{\mathrm{Re}(1/Y_{11})}. \quad (2)$$

Simulation and results. In this study, we simulated the proposed design using MATLAB software. The simulation results show a parametric study of conductor width w, the radius r of the TSV, and the number of turns N, to verify the extent to which structural parameters affect the electrical response of solenoid inductors. For a detailed examination of the effects of geometric parameters, we chose the frequency range 1–10 GHz as it includes the peak values of the electrical parameters (i.e., inductance and quality factor).

RDL width. As shown in Fig. 3, widening the width of RDL increases the quality factor with decreasing the value of the inductance due to the low resistance. At 6 GHz, the RDL width of 25 μm gives a maximum quality factor 50 and a minimum inductance 8,4 nH. Compared to a RDL width of 15 μm, it shows a 36 % variation in inductance and the Q factor decreases by 18 %.
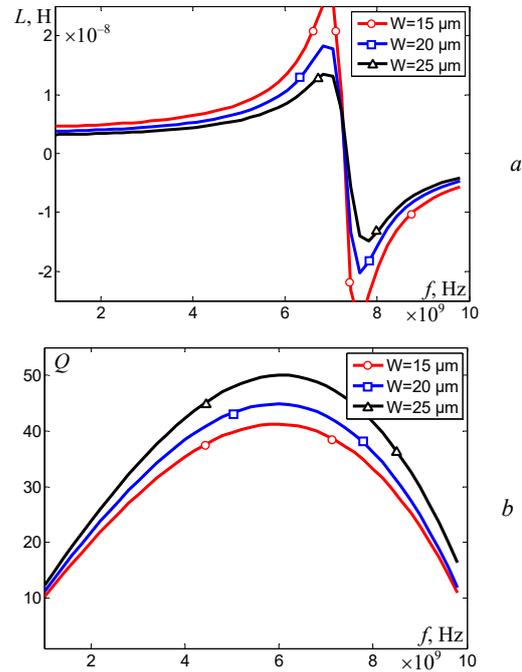

Fig. 3. Inductance (*a*) and quality factor (*b*) of TSV-inductor for different widths of RDL

Radius of TSV. Figure 4 shows the effect of changing the radius of the TSV while holding all other geometric parameters constant.

At 2 GHz, the smallest radius of 10 μm shows an inductance of 4.8 nH with a maximum difference of 31 %. The highest Q factor is observed in the largest diameter of 14 μm, which shows an improvement of 14 % compared to the smallest diameter. Therefore, to achieve a high inductance value with a high-quality factor, an optimum radius should be chosen.

Number of turns. Figure 5 shows the effect of changing N on inductance and quality factor while keeping all geometric parameters constant.

The inductance at 3 GHz is about 3.5 nH when the number of turns is 2 and increases to 5 nH when $N = 4$. With increasing frequency, we notice that there is a significant increase in inductance.

The quality factor peak at 49 when the number of turns is 2 at 7 GHz, for $N = 3$ the peak is 45 at 6.5 GHz, and for $N = 4$, is 42 at 6 GHz, respectively.
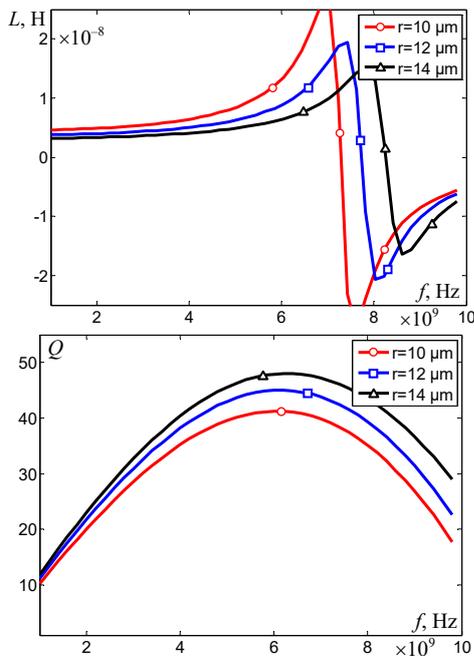
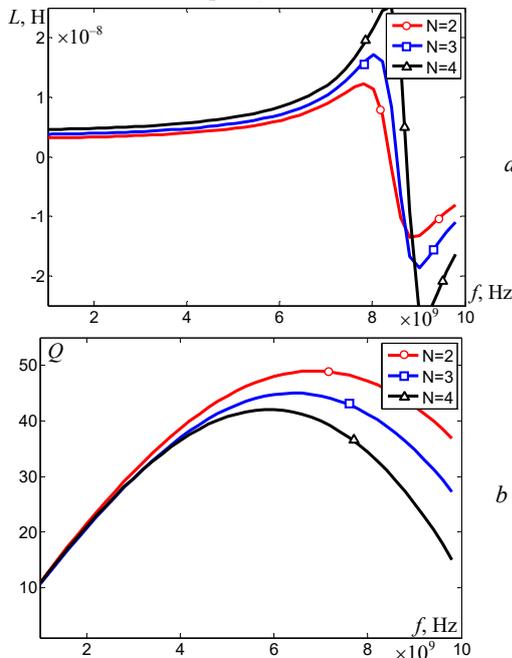Fig. 4. Effect of changing the radius of TSV on inductance (*a*) and quality factor (*b*)

Fig. 5. Inductance (*a*) and quality factor (*b*) for TSV-inductor against frequency from 2 to 4 turns

Comparison and application in buck converter. The results obtained from the proposed TSV-inductor are compared with the 2D inductors in Table 2.

Table 2
Comparison between spiral inductor, racetrack inductor and TSV-inductor

Reference	Type	Size, mm^2	L, nH	Q_{max}
[20]	Spiral inductor	26	13,84	16
[21]	Racetrack inductor	22,7	8,89	18
This work	TSV-inductor	**1,2**	**4,2**	**45**

It is clear that the proposed TSV-inductor in our work presents a higher quality factor compared to other conventional inductors. The low Q of the 2D inductors is caused by the large substrate loss. As shown in Table 2, the achieved quality factor in this work is greater than that

obtained in [20], [21] by 64,4 % and 60 %, respectively. The proposed inductor is considerably smaller than those of the other two types by about 95 %.

In order to compare the performance of the TSV-inductor with the other two types above, we applied each of them to a buck converter design with the same design specifications given in Table 3.

Table 3
Design specifications for the buck converter

V_{in}, V	V_{out}, V	f, MHz	Max load, A
1,5	0,8	500	0,5

Using a model of the TSV-inductor studied in the first part of this work in a buck converter gives the results obtained by the PSIM simulator. Figure 6 shows the output current of the buck converter at the frequency 500 MHz, which is stable at the value of 0,5 A after an initial period of about 2 ms. We also observe the same behavior for the output voltage shown in Fig. 7. It is noticeable that the input voltage decreased from 1.5 V to 0.8 V.
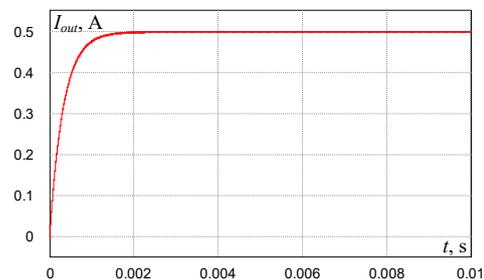

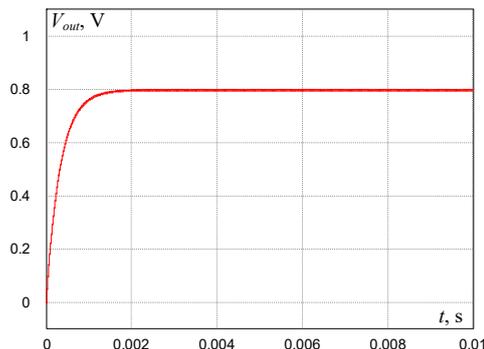Fig. 6. Current output of a buck converter using a TSV-inductor

Fig. 7. Voltage output of a buck converter using a TSV-inductor

A study of the effects of load current on the efficiencies of three designs was conducted. Figure 8 shows that all three designs achieve approximately the same efficiency between 0 and 100 mA, but the difference between them increases slightly after 150 mA and reaches 500 mA, which is the maximum load. As expected, the TSV-inductor improves its efficiency by up to 15 % and 6 % compared to the spiral inductor and racetrack inductor, respectively.
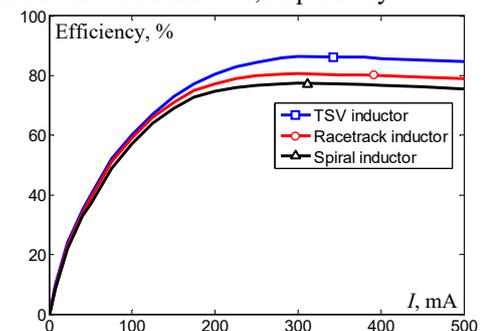

Fig. 8. Variation of buck converter efficiency as a function of load current for three inductors' different

Conclusions. In this article, a simple model of the through-silicon-via (TSV) inductor has been derived from the physical layout. Then, the effect of various geometric parameters such as the width of redistribution lines, the radius of TSV, and the number of turns was analyzed in detail using MATLAB simulations to determine the optimal TSV-indicator geometry parameters. Furthermore, we demonstrated the efficiency of the 3D TSV-inductor structure compared to other conventional 2D inductors in buck converter designs of the integrated circuit. According to simulations, the use of a TSV-inductor in a buck converter improves its efficiency by 15 % and 6 % compared to the spiral inductor and racetrack inductor, respectively. The results show that the TSV-inductor is a very promising approach for the integration of DC-DC converters.

Conflict of interest. The authors of the article declare that there is no conflict of interest.

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