Field programmable gate array hardware in the loop validation of fuzzy direct torque control for induction machine drive

Introduction. Currently, the direct torque control is very popular in industry and is of great interest to scientists in the variable speed drive of asynchronous machines. This technique provides decoupling between torque control and flux without the need to use pulse width modulation or coordinate transformation. Nevertheless, this command presents two major importunities: the switching frequency is highly variable on the one hand, and on the other hand, the amplitude of the torque and stator flux ripples remain poorly controlled throughout the considered operating speed range. The novelty of this article proposes improvements in performance of direct torque control of asynchronous machines by development of a fuzzy direct torque control algorithm. This latter makes it possible to provide solutions to the major problems of this control technique, namely: torque ripples, flux ripples, and failure to control switching frequency. Purpose. The emergence of this method has given rise to various works whose objective is to show its performance, or to provide solutions to its limitations. Indeed, this work consists in validation of a fuzzy direct torque control architecture implemented on the ML402 development kit (based on the Xilinx Virtex-4 type field programmable gate array circuit), through hardware description language (VHDL) and Xilinx generator system. The obtained results showed the robustness of the control and sensorless in front of load and parameters variation of induction motor control. The research directions of the model were determined for the subsequent implementation of results with simulation samples. References 19, tables 5, figures 26.

Key words: fuzzy control, field programmable gate array, Xilinx system generator, direct torque control, power system.
the IM for a defined operating condition. The IM model is used with measured variables to estimate stator flux and electromagnetic torque required by control diagram (Fig. 1), where $S_a$, $S_b$, $S_c$ are the Boolean switching commands; $\omega$ is the speed for reference speed $\omega_{ref}$; $E$ is the flux and torque error respectively; $T_e$ is the electromagnetic torque; $T_{eref}$ is the reference electromagnetic torque; $I_{sa}$, $I_{sb}$ are the stator currents in the abc reference frame; $\phi_{sref}$ is the reference stator flux; $|\phi_s|$ is the stator flux magnitude; $\theta_\phi$ is the stator flux angle.

Flux and torque estimation block based on CORDIC algorithm and Euler integration approach

Switching block

Speed Regulator

Fig. 1. DTC based IM control structure

The most significant element that can guarantee satisfactory DTC performance is stator flux estimator and torque estimator [12]. In this work we used optimized estimator developed in [14].

Fuzzy DTC based IM control structure. The research theme developed in this work mainly concerns the exploitation of new technological solutions to implement an intelligent control based on the DTC of an asynchronous machine around a hardware environment based on a FPGA.

This implementation is mainly aimed at reducing ripples at the level of electromagnetic torque and stator flux. In this part, two hysteresis regulators and Takahashi switching table (Table 1) will be replaced by a fuzzy controller. Figure 2 shows the control structure of fuzzy DTC based IM.

Fuzzy DTC control implementation. The hardware implementation of a fuzzy inference system consists in implementing 3 phases of a fuzzy logic regulation: fuzzification, fuzzy inferences and defuzzification. This principle is represented by Fig. 3.

Table 1

<table>
<thead>
<tr>
<th>$\phi$</th>
<th>$T_{es}$</th>
<th>$N$</th>
<th>$E_{ref}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>(1,0)</td>
<td>(1,1)</td>
<td>(0,1)</td>
</tr>
<tr>
<td>0</td>
<td>(0,1)</td>
<td>(1,1)</td>
<td>(0,0)</td>
</tr>
</tbody>
</table>

Description of fuzzification module. Fuzzification is the process of converting input data into fuzzy linguistic values. In literature, there are two material solutions to determine the degree of membership of a fuzzy set from a membership function.

The first solution is the memory-oriented approach, as the name suggests, for each finite number of inputs, the output values are calculated offline then they will be saved in memory. The advantage of this solution is that it is easy to change a membership function. The second solution is the calculation-oriented approach, only the
The characteristics of the membership functions are saved in a memory in order to simplify the on-line calculation of output values of each membership function. For the case of triangular membership functions, their characteristics are: the center of the triangle «c» and the slope «a».

The hardware implementation of this solution is a combinatorial circuit which can include adders, subtractors, multiplexers, multipliers and most of the time a control unit. In this study, we adopt the memory-oriented approach. Indeed, each linguistic input/output variable is represented by tables, a table for the degree of membership of each linguistic value. These tables are implemented in hardware by memory blocks ROMs addressable by a single input, such as the memory boxes which contain the degree of membership of linguistic value. However, the memory address space gives an image on the universe of discretized speech for example for a universe of normalized speech [0, 1] discretized in 64 points, we therefore use an address space [0: 63].

The membership functions of flux error, torque error, sectors and output vectors are illustrated by the following Fig. 4-7.

The hardware implementation of these functions is presented by hardware architectures in Fig. 8-11.
Rule inference and rule evaluation. Hardware description of fuzzy inference module is shown in Fig. 13. This module accepts as input three blocks of fuzzification module, the rule selector block allows building the rule base formed of 36 rules. This basis is obtained by making all the possible combinations between two fuzzy values of flux error, three fuzzy values of torque error and six fuzzy values of stator flux angle.

Composition of the rules. If several rules can be activated simultaneously and recommend actions with different degrees of validity on same output, we consider that the rules which are linked by an operator OR (Fig. 17)

\[ \mu_{By} = \max_i (\mu_{B_i}(y)) \quad i \in \{\text{indices of activated rules}\} \]

Description of defuzzification module. The hardware description of defuzzification module is carried out by a MAX operator as shown in Fig. 18. The inputs of this module are the outputs of the inference module. As it was specified in the preceding paragraph, the \(V_i (i = 0.7)\) correspond to the degree of activation of voltages \(V\). The output of this block, representing the output of the whole fuzzy block, corresponds to the voltage that it must be applied to the terminals of the machine through the inverter. The VHDL architecture of MAX defuzzification module is implemented by an assignment in the competitive mode:
Figure 18 shows a description of VHDL block used to implement the maximum defuzzification method.

**Simulation of fuzzy DTC control of asynchronous machine.** This phase involves the integration of a fuzzy inference system into DTC control algorithm. In this part, similarly to simulation with MATLAB, we will simulate using Xilinx generator system the architecture of the conventional DTC control and fuzzy DTC control. The fuzzy DTC control is applied to an IM whose specifications are given in Table 2.

<table>
<thead>
<tr>
<th>IM parameters</th>
<th></th>
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<tbody>
<tr>
<td>Nominal voltage $U_n$, V</td>
<td>220</td>
</tr>
<tr>
<td>Nominal current $I_n$, A</td>
<td>2.35</td>
</tr>
<tr>
<td>Mechanical power $P_n$, kW</td>
<td>1.08</td>
</tr>
<tr>
<td>Nominal speed $N$, min⁻¹</td>
<td>1430</td>
</tr>
<tr>
<td>Supply frequency $f$, Hz</td>
<td>50</td>
</tr>
<tr>
<td>Stator resistance $R_s$, Ω</td>
<td>10</td>
</tr>
<tr>
<td>Rotor resistance $R_r$, Ω</td>
<td>6.3</td>
</tr>
<tr>
<td>Stator self inductance $L_s$, H</td>
<td>0.4642</td>
</tr>
<tr>
<td>Rotor self inductance $L_r$, H</td>
<td>0.4612</td>
</tr>
<tr>
<td>Mutual inductance $L_m$, H</td>
<td>0.4212</td>
</tr>
<tr>
<td>Moment of inertia $J$, kg·m²</td>
<td>0.02</td>
</tr>
<tr>
<td>Pole pairs number $p$</td>
<td>2</td>
</tr>
</tbody>
</table>

The structure of conventional DTC control is illustrated in Fig. 1. Regarding fuzzy DTC control shown in Fig. 2, we will replace the blocks of hysteresis comparator modules and DTC control selection table by a fuzzy inference system that we have built and tested. To compare the both control approaches, we simulated these modules on MATLAB / Simulink with Xilinx generator system. The results are illustrated in Fig. 19.

Note that there is an improvement in the electromagnetic flux and torque obtained by the fuzzy DTC control compared to that obtained with the conventional DTC control with a significant reduction in ripples. Table 3 shows the performance in terms of resource consumption, obtained during the implementation of architecture of fuzzy DTC control on VIRTEX 4 FPGA given by architecture presented in Fig. 2.

**Table 2**

We note that the proposed architecture optimizes the use of the hardware resources of FPGA card (10 % of Slices and 7 % of LUTs), moreover this architecture considerably reduces the logical components used compared to architectures presented in [15, 16].

The maximum clock frequency is set by the synthesis tool equal to 231.64 MHz, which corresponds to a minimum period of 4.317 ns. In contrast, in [16] the maximum clock frequency is 54 MHz using DSPACE (Digital Signal Processing and Control Engineering). In [17] the minimum period is equal to 50 ns. We see that execution time is too long compared to FPGA due to sequential processing of DSPACE.

Table 4 presents the hardware resources consumed in this architecture compared to previous work in the same research axis.

**Table 3**

**Table 4**

<table>
<thead>
<tr>
<th>Logic utilization</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA device family</td>
<td>[7] [18] [19] [14] Proposed</td>
</tr>
<tr>
<td>Xilinx Virtex-4</td>
<td>10.346 6.931 3.256 2.909 2.836</td>
</tr>
<tr>
<td>Altera DE-115</td>
<td>80 57  – – –</td>
</tr>
<tr>
<td>Altera CYCLONE II</td>
<td>18.594 6.491 2.549 7.411 7.686</td>
</tr>
<tr>
<td>Xilinx Virtex-4</td>
<td>12 192 6 %</td>
</tr>
<tr>
<td>Xilinx Virtex-4</td>
<td>4 32 12 %</td>
</tr>
</tbody>
</table>

**Fig. 18. VHDL MAX defuzzification module**

**Fig. 19. Electromagnetic torque and stator flux obtained by XSG simulator for DTC (a) and fuzzy DTC (b)**
Validation of hardware architecture of proposed fuzzy controller. After simulation step, the proposed hardware architecture of fuzzy controller was validated by co-simulation hardware on the ML402 target peripheral equipped with a VIRTEX4 FPGA circuit.

This step is dedicated to implement the control algorithms on a development board integrating an FPGA component. It is mainly intended for the verification and validation of digital implementation of control algorithms on FPGA targets in «Hardware in the loop» simulation environment as shown in Fig. 20.

Fig. 20. Hardware in the loop validation of fuzzy DTC controller

Once simulation and timing analysis are done, the procedure of hardware co-simulation in XSG makes a bitstream file from the hardware prototype and a point to point Ethernet block for Hardware-In-the-Loop (HIL) procedure (Fig. 21).

Fig. 21. Fuzzy DTC HIL point to point Ethernet block

The created block (Fig. 20) substitutes the architecture hardware that was constructed before (fuzzy DTC).

The point-to-point Ethernet blocks are linked to inverter and IM to run a HIL (Fig. 22). In this situation the models of motor and inverter are simulate in MATLAB/Simulink environment, and XSG architectures of Fuzzy DTC are achieved in the ML402 FPGA device. The HIL validation is executed by connecting the target device to PC via an Ethernet cable.

The spectral analysis by MATLAB with Powergui FFT analysis tool of electromagnetic torque obtained by conventional DTC (Fig. 24) proposed in [14], the neuronal DTC (Fig. 25) proposed in [7] and by fuzzy DTC (Fig. 26) in steady state shows the existence of harmonics along the spectrum of electromagnetic torque obtained by conventional DTC unlike electromagnetic torque obtained by Fuzzy DTC. Table 5 shows the root mean square (RMS) error and the maximum ripple band of electromagnetic torque and stator flux for conventional DTC, the neuronal DTC and fuzzy DTC approaches.

The results of Table 5 show that DTC based on intelligent techniques considerably reduces the ripples of electromagnetic torque and stator flux compared to conventional DTC. Fuzzy DTC architecture gives the best results in terms of hardware resource consumption and in terms of electromagnetic torque ripple elimination.
Conclusions.

1. The aim of this work was, first of all, to improve the dynamic performance of the direct torque control applied to induction motor supplied by a voltage inverter by introducing of a fuzzy inference system. Secondly, to materialize the feasibility and to judge the quality of proposed control.

2. In this article, we mainly describe the development, implementation and validation of hardware architecture on field programmable gate array for fuzzy direct torque control of induction motor.

3. The originality of this work has been to combine the performance of artificial intelligence techniques and execution power of programmable logic circuits, for the definition of a control structure achieving the best simplicity / performance and speed / performance ratios.

4. We used unconventional control tools to implement a switching strategy without needing the switching table and hysteresis comparators used in conventional direct torque control.

5. Finally, we believe that the proposed solution improved the dynamic performance of induction motor and greatly reduced the disadvantages of conventional direct torque control such as torque ripples, flux ripples and switching frequency.

Conflict of interest. The authors declare that they have no conflicts of interest.

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Received 25.07.2022
Accepted 15.11.2022
Published 06.05.2023

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How to cite this article:

Received 25.07.2022
Accepted 15.11.2022
Published 06.05.2023

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How to cite this article:

Received 25.07.2022
Accepted 15.11.2022
Published 06.05.2023

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