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Investigation of efficient multilevel inverter for photovoltaic energy system and electric vehicle applications

Introduction. *This research presents a simple single-phase pulse-width modulated 7-level inverter topology for renewable system which allows home-grid applications with electric vehicle charging. Although multilevel inverters have appealing qualities, their vast range of application is limited by the use of more switches in the traditional arrangement. As a result, a novel symmetrical 7-level inverter is proposed, which has the fewest number of unidirectional switches with gate circuits, providing the lowest switching losses, conduction losses, total harmonic distortion and higher efficiency than conventional topology.* ***The novelty*** *of the proposed work consists of a novel modular inverter structure for photovoltaic energy system and electric vehicle applications with fewer numbers of switches and compact in size.* ***Purpose.*** *The proposed system aims to reduce switch count, overall harmonic distortions, and power loss. There are no passive filters required, and the constituted optimizes power quality by producing distortion-free sinusoidal output voltage as the level count increases while reducing power losses.* ***Methods.*** *The proposed topology is implemented with MATLAB/Simulink, using gating pulses and various pulse-width modulation methodologies. Moreover, the proposed model also has been validated and compared to the hardware system.* ***Results****. Total harmonic distortion, number of power switches, output voltage, current, power losses and number of DC sources are investigated with conventional topology.* ***Practical value.*** *The proposed topology has proven to be extremely beneficial for implementing photovoltaic-based stand-alone multilevel inverter and electric vehicle charging applications.* References 16, table 1, figures 18.

Key words: **conduction loss, multilevel inverter, pulse-width modulation, switching loss, total harmonic distortion.**

Вступ*. У цьому дослідженні представлена топологія простого семирівневого однофазного інвертора з широтно-імпульсною модуляцією для системи з відновлюваними джерелами енергії, яка дозволяє використовувати домашню мережу з зарядкою електромобілів. Хоча багаторівневі інвертори мають привабливі характеристики, широкий спектр їх застосування обмежений використанням більшої кількості перемикачів у традиційній схемі. В результаті запропонований новий симетричний 7-рівневий інвертор, який має найменшу кількість односпрямованих ключів із затворними ланцюгами, забезпечує найменші комутаційні втрати, втрати на провідність, сумарні гармонічні спотворення та вищий ККД, ніж традиційна топологія.* ***Новизна*** *запропонованої роботи полягає у новій модульній структурі інвертора для фотоелектричних енергетичних систем та використання для електромобілів з меншою кількістю перемикачів та компактними розмірами.* ***Мета****. Пропонована система спрямована на зменшення кількості перемикань, загальних гармонічних спотворень та втрат потужності. Пасивні фільтри не потрібні, а складова частина оптимізує якість електроенергії, створюючи синусоїдальну вихідну напругу без спотворень зі збільшенням кількості рівнів при одночасному зниженні втрат потужності.* ***Методи****. Запропонована топологія реалізована за допомогою MATLAB/Simulink з використанням стробуючих імпульсів та різних методологій широтно-імпульсної модуляції. Крім того, запропонована модель також була перевірена та порівняна з апаратною системою.* ***Результати****. Загальні гармонічні спотворення, кількість силових ключів, вихідна напруга, струм, втрати потужності та кількість джерел постійного струму досліджуються за допомогою традиційної топології.* ***Практична цінність****. Запропонована топологія виявилася надзвичайно корисною для реалізації автономних багаторівневих інверторів на основі фотоелектричних систем та застосування для заряджання електромобілів.* Бібл. 16, табл. 1, рис. 18.

Ключові слова: **втрати провідності, багаторівневий інвертор, широтно-імпульсна модуляція, комутаційні втрати, сумарні гармонічні спотворення.**

Introduction. The power grid has experienced energy requirements since the last century due to the growing number of users along with large power companies. Due to the obvious advancements in semiconductor device development, power converter technology is rapidly transforming the way traditional large transformers. So, order to offer clean electricity to users, power converters are frequently employed in renewable energy conversion systems. Switching devices are economical to produce and maintain a competitive advantage because of their minimal costs. Because adding additional switches to an inverter circuit does not considerably increase prices, 2-level traditional converters having large power losses and harmonics content are increasingly becoming substituted by multilevel converters with lower operating frequencies.

Many studies have concentrated on the creation of multilevel inverters (MLIs), including both terms of topologies and control technique. The number of elements used in these sorts of converters is given special consideration. The fewer the elements, the lesser the power dissipation and expenses. Cascaded H-bridge, neutral point, and cascaded H-bridge are some of its most prevalent structures. MLIs with clamped and diode clamped diodes have discovered significant practical demand for high variable speed drives. Additional ripple losses are attributed to presence of clamped diodes and capacitors. Consequently, as compared to cascaded modified MLI, which uses diodes and capacitors, it is a much more complex topology [1-4].

Single-phase MLIs can play an important role in this area, converting the photovoltaic (PV) system's DC voltage into a continuous AC signal accessible by loads as well as the gird significantly fewer harmonic filters and increased performance. The 7-level power conditioning unit inverter has been proposed for this purpose, with appealing features such as low number of switches and the ability to generate multiple voltage ranges at the result [5, 6].

Modified MLI designs based on a decreased number of circuit elements are implemented to tackle the previous shortcomings. In this research, a 7-level pulse-width modulation (PWM) inverter with independent DC input supplies and appropriate circuit combinations for switches and total harmonic distortion (THD) minimization is proposed. Furthermore, it necessitated a greater switching devices and external power supply, resulting in a larger inverter size and expense. In order to reduce the amount of power devices and converter losses, a staircase MLI is proposed [7-9].

This configuration, on the other hand, takes into account something even increasing switching devices. The quantity of external DC sources is decreased due to the absence of voltage multiplication across input split-capacitors. This configuration, on the other hand, can be employed for up to 5 levels of composition without the need for flexible modification. MLI with decreased switches is offered for some further switching minimization, but output voltage generation takes a massive number of discrete DC sources [10, 11].

For low voltage PV panels, a new single-phase MLI inverter featuring wattage capabilities was proposed. It is, therefore, appropriate for low rated power applications and has 2 adapt an appropriate, resulting in increased power losses. For cascade multilevel output-voltage, a small MLI is given employing 2 capacitors within every component and a decrease in number of external power supply. However, for high-power applications, this boosts inverter energy capacity and compact. For energy storage systems, novel MLI topologies for single/3-phase applications with fewer components and a single DC-source are required [12-16].

Inspired by an analysis of relevant literature, this research introduces single-phase 7-level PWM inverter with decreased power number of switches, THD, switching losses, and conduction losses for stand-alone grid-integrated PV systems and electric charging applications. The suggested inverter minimises the needed amount of parts to a competitive level in order to increase efficiency, footprint, and cost. The primary and secondary networks of the intended MLI are separated. The primary circuit is a simple H-bridge inverter that controls output voltage orientation, while the supplementary circuit is a series of switching that generate every output voltage level. The PV fed proposed MLI application in domestic and electric vehicle (EV) charging is shown in Fig. 1.

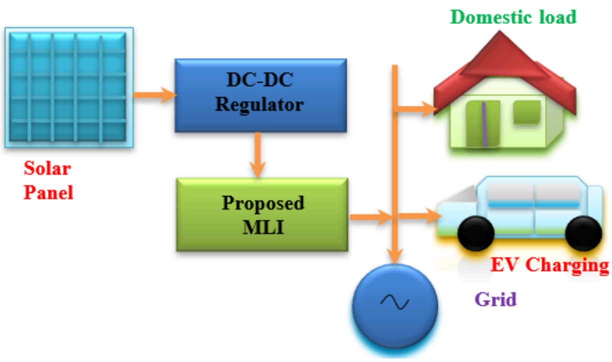

Fig. 1. PV fed proposed MLI application in domestic and EV charging

Proposed topology and modes of operation. In a traditional topology, a cascaded H-bridged MLI has 3 DC sources and 3 H-bridge units, typically having switching devices, for a total of 12 switches: $L = (S+2)/2$, where S is the number of switches and L is the level of output voltage in steps in the configuration. Each bridge produces 3 levels: $+V_{dc}$, $0V_{dc}$, and $0V_{dc}$. Generating stepped 7 level staircase wave patterns by cascading 3 bridges in this manner. In a suggested MLI, 10 number of switching devices and 3 DC sources have been included (Fig. 2).

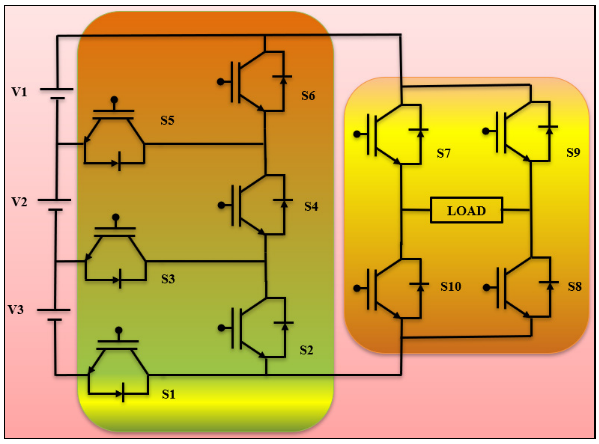

Fig. 2. Proposed topology of MLI

Throughout mode I operation, the output voltage has been determined, which is $+V_{dc}$ (Fig. 3); similarly, during mode II operation, input DC voltages are added by 2 number of DC sources, resulting in an output voltage of $+2V_{dc}$; and finally, a positive third level of voltage has to be estimated, which is $+3V_{dc}$ (Fig. 4, 5). Furthermore, using the equivalent circuits of Fig. 6–8, the negative sequence of output voltage levels of $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$ has been determined. Figure 9 shows that the proposed inverter combines a multicarrier PWM technique to verifying 7 levels, 6 different triangular waves, and one reference wave signal to produce switching patterns.

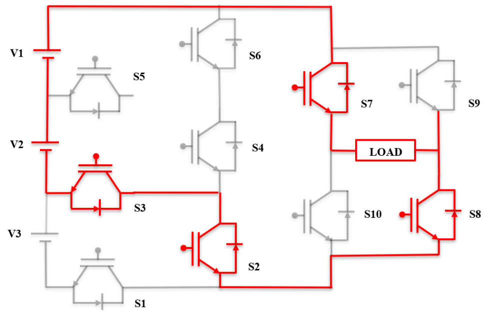

Fig. 3. Mode I operation

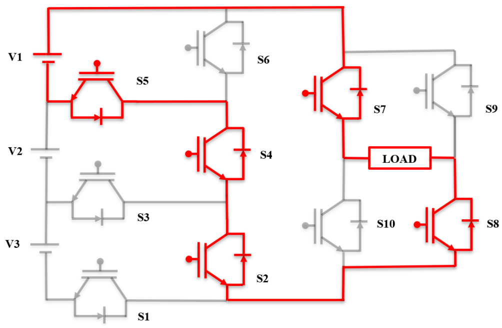

Fig. 4. Mode II operation

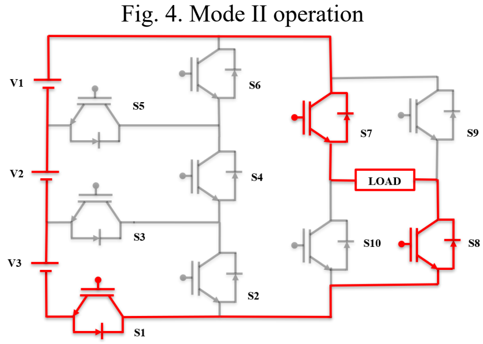

Fig. 5. Mode III operation

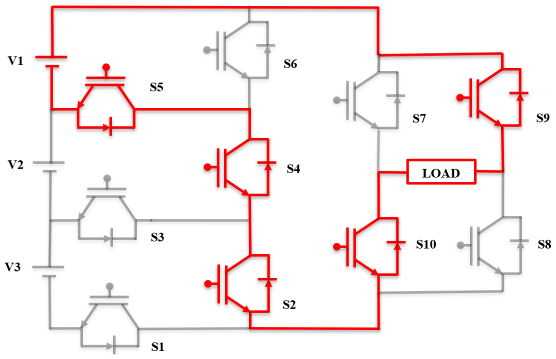

Fig. 6. Mode IV operation

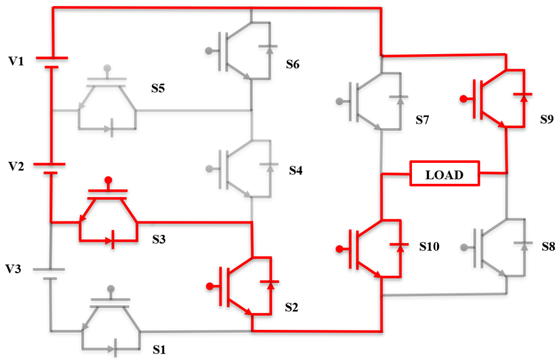

Fig. 7. Mode V operation

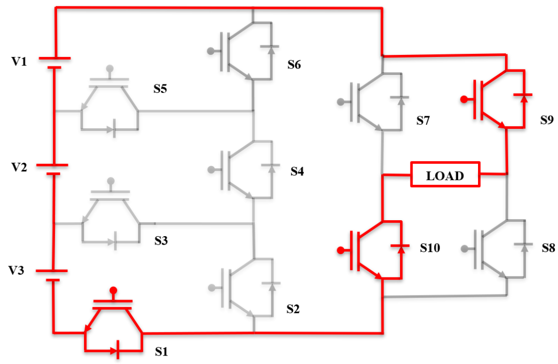

Fig. 8. Mode VI operation

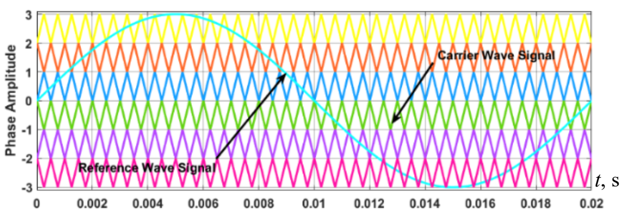

Fig. 9. Sinusoidal PWM for generating switching pulses

Results and discussion. The output voltage and current of the proposed MLI with a resistance of 100 Ω are shown in Fig. 10, 11 respectively. Since output current precedes output voltage, these 2 waveforms are nearly symmetrically maintained. Figure 12 shows the results of a THD investigation of an inverter with resistive load; the THDs collected have a similar pattern due to the unique wave pattern. The output voltage and current of the proposed MLI for resistance values of 100 Ω and 25 mH are shown in Fig. 13, 14. The output current pattern changes due to the inductance feature, hence these 2 waveforms are distinct. Figure 15 shows the results of an inverter's THD assessment under resistance and inductive load.

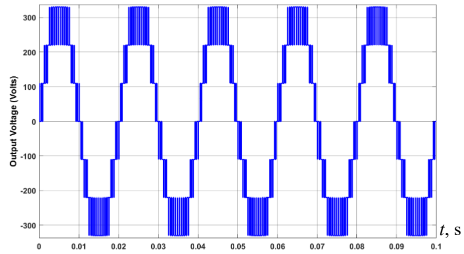

Fig. 10. Output voltage of proposed MLI for resistive load

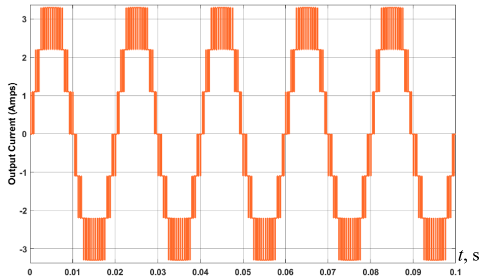

Fig. 11. Output current of proposed MLI for resistive load

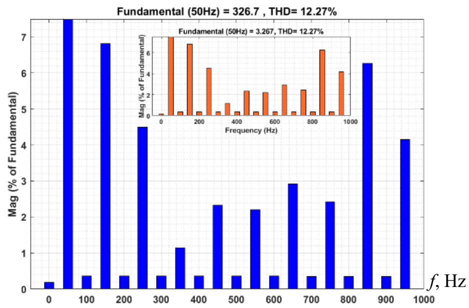

Fig. 12. THD analysis of proposed MLI during resistive load

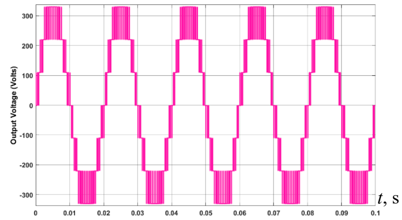

Fig. 13. Output voltage of proposed MLI for *RL* load

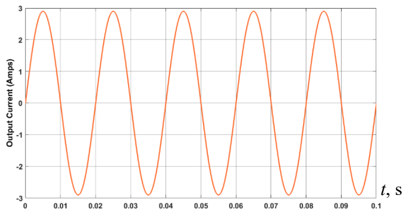

Fig. 14. Output current of proposed MLI for *RL* load

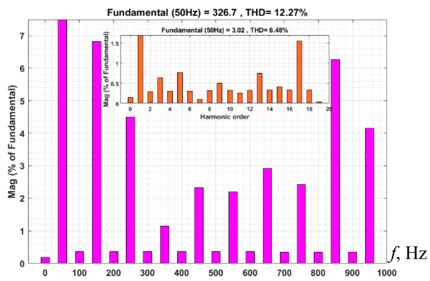

Fig. 15. THD analysis of proposed MLI during *RL* load

Power loss and efficiency. The modulation index of PWM signal is evaluated as:

$$A_m = F_m / F_r \,, \quad (1)$$

where F_m and F_r are represented as the modulated and reference signals respectively.

Voltage THD of proposed MLI is calculated by (2), in the same manner current harmonics also calculated as:

$$THD = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}{V_1}}, \qquad (2)$$

where V_1 is the fundamental root mean square (RMS) voltage; V_2, ..., V_n are the RMS voltage of the n^{th} harmonics. In the similar manner current total harmonics also calculated.

The losses in the developed proposed structure are mostly intense on 3 main power losses, specifically losses during switching ($W_{Switching}$) and conduction ($W_{Conduction}$). Then overall power loss (W_{Loss}) of MLI is:

$$W_{Loss} = W_{Switching} + W_{Conduction}. \qquad (3)$$

Conduction loss of power semiconductor devices is:

$$W_{Conduction} = \int_0^{T_0/2} \left\{ \begin{aligned} &\left[V_{CE0} + r i_p \sin \omega t\right] \times \\ &\times i_p \sin \omega t \left[\frac{1}{2}\left(1 + A_m \sin(\omega t + \varphi)\right)\right] \mathrm{d}t \end{aligned} \right\},$$

where V_{CE0} is the zero-current collector to emitter voltage; r is the collector to emitter on-state resistance; A_m is the modulation index; i_p is the peak current of IGBT device.

After simplification we have:

$$W_{Conduction} = \frac{1}{2} \left\{ \begin{aligned} &\left(V_{CE0} \frac{i_p}{\pi} + r \frac{i_p^2}{4} \right) + \\ &+ \left(A_m \cos \varphi \cdot V_{CE0} \cdot \frac{i_p}{8} \right) + \left(\frac{1}{3\pi} r i_p^2 \right) \end{aligned} \right\}. \qquad (4)$$

Switching loss is expressed as the integration of all the turn-on and turn-off switching energies at the switching instants. In the equation, variable switching time is considered and integrated as:

$$W_{Switching} = f_{sw} \frac{1}{T_0} \int_0^{T_0/2} \left(E_{on} + E_{off}\right) \cdot \left(t, i_p\right) \mathrm{d}t, \qquad (5)$$

where T_0 is the switching time period; f_{sw} is the switching frequency; E_{on} is the on-state voltage drop; E_{off} is the off-state voltage drop.

The efficiency of MLI is calculation as:

$$Efficiency = \frac{P_{Output}}{P_{Output} + W_{Loss}} \cdot 100\%. \qquad (6)$$

Experimental setup and validation. A prototype of a symmetric 7-level inverter was examined under various loading conditions as well as dynamic variations in load values by setting the modulation index to value of 1. The MLI configuration consists of 2 DC sources (V_{dc} = 75 V) and 10 IGBT switches which produces 7-level output with the maximum value of 326 V. The other parameters are considered as follows: FGA25N120 IGBT switch, TLP350 driver circuit, R load value is 100 Ω and RL load value of R = 100 Ω, L = 25 mH and the triggering signal for the IGBT switches is produced by the real-time controller dSpace1104 in real time. The carrier switching frequency is applied for the value of 2 kHz. Figure 16 depicts an experimental arrangement of proposed 7-level inverter. The output voltage THD is 16 % and fundamental peak voltage of 326 V for the RL load (R = 100 Ω and L = 240 mH). Figure 17, 18 show the 7-level voltage pattern and current THD is 8 %.

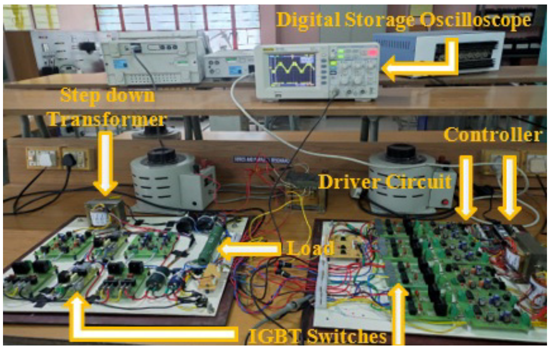

Fig. 16. Experimental setup of proposed MLI

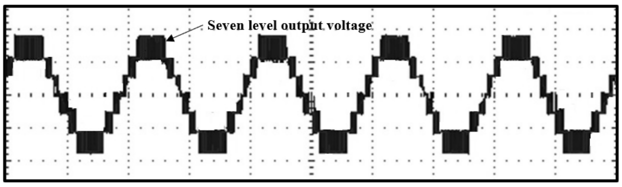

Fig. 17. Output voltage of proposed MLI

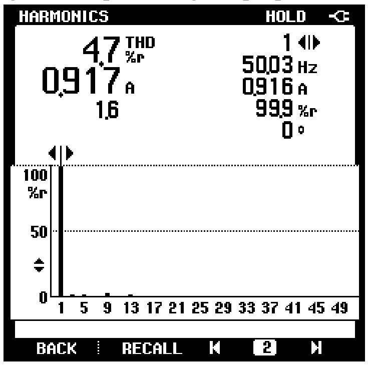

Fig. 18. THD analysis of proposed MLI (current)

While considering AC voltages from same DC source, voltage gain produced from both topologies are same. Proposed converter having the features of more DC link voltage utilization, lower voltage stress and total standing voltage is less. If output power from existing topology THD of voltage and current value obtained as 12.27 % and 8 % during different loads. The designed prototype converter with specification of 325 V is achieved THD value of 8.3 %. Comparison between traditional and proposed converter is given in Table 1.

Table 1

Comparison between traditional and proposed 7-level MLI

Parameters	Conventional topology	Proposed topology
Number of power switches	12	10
Load type	R = 100 Ω	R = 100 Ω
	R = 100 Ω; L = 25 mH	R = 100 Ω; L = 25 mH
Symmetric supply voltage, V	75	75
Number of DC sources	3	3
Modulating frequency f_m, Hz	50	50
Carrier frequency f_c, Hz	2000	2000
Output voltage, (peak value, V)	326.7	326.7
Output current, A	3.26 (R load) 3.04 (RL load)	3.26 (R load) 3.02 (RL load)
Switching losses	0.325	0.121
Conduction losses	48.42	46.75
Power losses	48.86	46.87
Efficiency	94.29	96.25
% THD (voltage)	12.27	12.27
% THD (current)	8.3	6.48

Efficiency and THD values show proposed converter with prototype model is better than traditional converter so efficiency of proposed converter is 96.25 %. Due to less THD 8.3 % than traditional, so proposed converter have more efficiency than traditional converter.

5. Conclusions. Proposed single-phase 7-level inverter is developed with lesser number of switches and it fulfill the needs of the MLI. Proper control signal is applied to the switches in the correct sequence; proposed single-phase 7-level inverter produced 7-level of AC output. Based on the operation of reference and carrier wave signal, power semiconductor switches are controlled in efficient manner. Proposed single-phase 7-level inverter operation is initially developed and investigated in MATLAB/Simulink tool and same to be validated in real-time proto-type hardware. THD values obtained between the ranges 8 % with 3 different loads in hardware level. Efficiency of proposed converter is obtained as 96.25 %. From the comparisons proposed single-phase 7-level inverter is much better than traditional converter in both symmetric and asymmetric topology.

Conflict of interest. The authors declare that they have no conflicts of interest.

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