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AN EFFECTIVE CONTROL ALGORITHM FOR DYNAMIC VOLTAGE RESTORER UNDER SYMMETRICAL AND ASYMMETRICAL GRID VOLTAGE CONDITIONS

Introduction. Voltage sag, which is associated to a transitory drop in the root mean square voltage characterizing an electrical source network. During these perturbations, the corresponding electronic customers and devices will suffer from serious operating troubles causing dangerous damages. **Purpose.** In order to attenuate this disturbance effects, the Controlled Dynamic Voltage Restorer constitutes a very interesting solution among many others that have been proposed. **The novelty** of the proposed work consists in presenting an enhanced algorithm to control efficiently the dynamic voltage restorer when voltage sag is suddenly occurred. **Methods.** The proposed algorithm is based on an instantaneous phase locked loop using a multi variable filter to synthesize unitary signals involved in compensation voltages computation relative to the sag apparition. **Practical value.** A detailed study concerning typical voltage sag, which is consolidated by simulation and experimental results, is conducted to show the used algorithm's effectiveness to cancel the corresponding voltage sag. References 44, table 1, figures 16.

Key words: dynamic voltage restorer, power quality, voltage sag, phase locked loop, synchronous reference frame.

Вступ. Провал напруги, який пов'язаний із тимчасовим падінням середньоквадратичної напруги, характеризує мережу джерел електричної енергії. Під час цих збурень відповідні споживачі (електронні прилади та інші пристрої) будуть страждати від серйозних проблем у їхній експлуатації, що спричиняють небезпечні пошкодження. **Призначення.** Для того, щоб послабити вплив цих збурень, контрольований динамічний відновник напруги видається дуже цікавим рішенням серед багатьох інших, які були запропоновані. **Новизна** запропонованої роботи полягає у представленні вдосконаленого алгоритму ефективного управління динамічним відновником напруги, коли раптово відбувається провал напруги. **Методи.** Запропонований алгоритм базується на миттєвому фазовому замкненому контурі з використанням багатоваріантного фільтра для синтезу унітарних сигналів, що беруть участь у обчисленні напруги компенсації стосовно прояву провалу. **Практичне значення.** Детальне дослідження стосовно типового провалу напруги, яке узгальнено за допомогою моделювання та експериментальних результатів, проведено, щоб показати ефективність використовуваного алгоритму для ліквідації відповідного провалу напруги. Бібл. 44, табл. 1, рис. 16.

Ключові слова: динамічний відновник напруги, якість електроенергії, провал напруги, фазовий замкнений контур, синхронна система відліку.

1. Introduction. Power distribution system is an irreplaceable thing. Indeed, it should provide energy for costumers in an ideal sinusoidal form. For that, the number of connected equipments to the power network still increasing but that fact imposes critical problems to the network [1–3]. Poor power quality outcomes in financial losses which has a major harmful impact on the economical industry sector.

The voltage quality issues is more important in comparison to sensitive loads which requires to be supplied cautiously, regarding to the previous mentioned problem, it consist mainly in voltage sags and swells, voltage harmonics, current harmonics, fluctuations (flickers), frequency variation and unbalance [4–7].

Voltage sag has been widely studied in a considerable research papers, which is defined as temporary decrease in the root mean square voltage between 10 to 90 % of nominal voltage, for a duration interval of 0.5 cycles to one minute as it's presented in IEEE 1346, IEEE 1159 and IEC 61000-2-1 standers [8, 9]. By way of explanation it is characterized by a sudden reduction of nominal voltage from 0.1 to 0.9 per unit followed after a short period of time by a voltage recovery. According to the mentioned standards, normal voltage sag takes from 10 ms to 1 minute.

Voltage sags caused mainly by large induction motors starting or by different faults related to power system. Consequentially, sensitive loads and a significant number of electronic devices could be malfunctioned or completely deteriorated as a result for voltage sag occurrence. Hence, huge losses at costumer loads are take place.

Voltage swell is defined in the previous mentioned IEEE standard as an increase in the root mean square (RMS) supply voltage from 1.1 to 1.8 per unit for duration from 0.5 cycles to 1 min. Voltage swell are mainly due to large capacitors switching or connecting / disconnecting of heavy loads. Voltage swells are less widespread in distribution network, for that reason, they are not as important as voltage sags [10–14].

The above mentioned issues related to power quality has opened up a discussion on possible solutions to overcome these problems. Researchers have proposed a large number of custom power devices (CPDs). The most effective one is to use compensators based on power electronic devices.

These compensators could be in series, shunt or hybrid form. Literature is rich by numerous classifications of CPD [15], Based upon its structure, various custom power devices are usually classified into three categories: unified power quality conditioners (UPQC), distribution static compensator (D-STATCOM) and dynamic voltage restorer (DVR).

Using series or shunt power filters in separate may not be the wanted preferred solution. For this reason, the device named UPQC [16, 17] performing both functionalities of series and shunt active filter is introduced and its concept is developed [18, 19].

The D-STATCOM is another choice for solving voltage unbalance, and power quality enhancement. It maintains the voltage sag at the desired reference by supplying or receiving the reactive power in the distribution

network. This compensator has been deployed in a three-phase four-wire distribution system [20].

Another alternative based on series custom power compensation could ensure a high quality voltage purpose [12, 13]. DVR is composed of a dc-energy storage system, a voltage source converter, an output filter and a coupling transformer.

The performance of the abovementioned CPDs is related mainly to the control algorithm of each device. Indeed, researchers pay a great attention to the algorithm strategies. Instantaneous Symmetrical Components Theory (ISCT) generates reference waveforms to balance a given load [21, 22]. Instantaneous Power Theory is introduced to compensate voltage faults in a dynamic way in the time domain based on PQR transformation [23]. Adaline (Adaptive linear element) control strategy is an Artificial Neural Network (ANN) that is used to control a capacitor supported DVR for power quality enhancement [24]. Space Vector PWM Strategy is presented in [25] to control a modified DVR composed of a conventional three phase voltage source inverter and an emitter follower. Synchronous Reference Frame Theory [26] is one of the most used algorithms to generate reference signals; its operating principle is based mainly on converting the load voltages to the rotating reference frame using the Park's transformation with unit vectors derived by a phase locked loop (PLL).

Detecting the grid phase angle and frequency in a fast and accurate way is the key of a good synchronization process. Several synchronization methods have been proposed in literature; the method based on detecting the zero crossing point of the grid voltages is characterized by a large synchronization time. In addition, it fails in detecting that point in case of grid frequency variation and unbalanced voltages.

The algorithm based on $\alpha\beta$ stationary reference frame conversion [27] is another alternative to detect the grid phase angle and frequency. The algorithm performances are related mainly to the intrinsic filter parameters that affect the algorithm dynamic response under asymmetrical grid faults conditions.

In three phase application, the phase locked loop (PLL) is the most used strategy where the synchronous reference frame (SRF) based PLL constitutes the common configuration [28–30]. It based on transforming the three phase voltages from abc frame to synchronous rotating reference frame using Park's transformation in order to identify the grid angle and frequency quantities.

Synchronous Reference Frame is known as a feed forward open loop control strategy. It is characterized by its simplicity and stability. Their main inconvenient is expressed in poor transient response and possibility offset error at the steady state because of voltage drop on the injection transformer and the series branch of the filter. To overcome these problems, feedback controllers are used. Feedback control process consists of measuring the DVR output voltages and fed back to the controller voltages. A variety of controllers have been presented in literature such as proportional, Proportional-Integral (PI), Proportional-resonant (PR) [31, 32], fuzzy controller [33, 34], H_∞

controller [35], sliding mode controller [36–38], state variable controller [39], predictive and repetitive controllers [40–42], feedback linearization [43].

The goal of the paper is the investigation of an effective phase locked loop to generate unitary signals that contain the fundamental voltage phase angle information used in calculating compensating voltage in case of a voltage sag occurrence.

Subject of investigations. The introduced PLL is compared to the conventional one in simulation and experiment. After that, controlling the DVR by the proposed algorithm is accomplished to show the effectiveness of the algorithm.

This paper is structured as follows: Section 2 describes the Dynamic Voltage Restorer Configuration topology with its operating principle with respect to sudden voltage sags occurring. Section 3 presents the control algorithm explaining both conventional phase locked loop topology and the proposed one. Section 4 discusses the obtained results through simulation and experimentation studies. Finally, a conclusion relative to the obtainable work is presented.

2. DVR Configuration Topology. A dynamic voltage restorer is generally connected in series with the protected load through a transformer. A DVR generates voltage references to be added to those of the grid in order to compensate the voltage disturbance at the load side. The schematic configuration of a typical DVR is presented in Fig. 1, which contains the following elements:

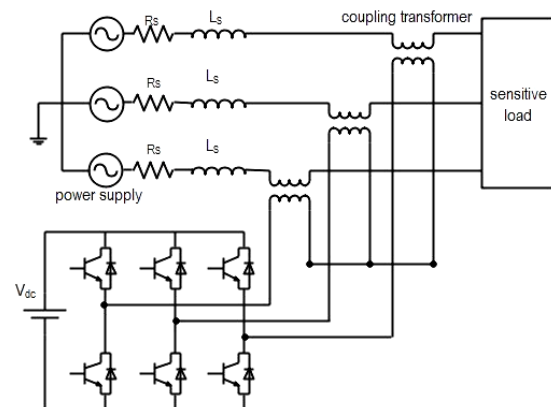


Fig. 1. DVR Schematic Topology

1) *Energy storage device*: commonly called DC bus side, it allows the voltage source inverter to provide the power grid by the reference generated voltages via the transformer. It could be batteries, capacities or even photovoltaic panels.

2) *Voltage Source Inverter (VSI)*: a voltage source inverter is a power electronic configuration fed by the previously mentioned energy storage device to regenerate the desired sinusoidal voltage references. Recently, the switching configuration of the Voltage Source Inverter is based on IGBT. Nevertheless, peaks due to the switching process are eliminated by passive elements such as resistance R , inductance L , and a capacitance C at the VSI output.

3) *Injection transformer*: the main purpose of this transformer is to inject the generated voltage references to

the power grid which is connected by its high voltage side, whereas, the low voltage side is connected to the DVR power circuit.

4) *Control strategy*: control algorithm is considered as DVR heart. definitely, it detect the voltage disturbance and generate a voltage reference in phase to those of the grid and control the Voltage Source Inverter by generated voltage in feedback control in order to compensate the occurred voltage disturbance.

DVR could be expressed in an equivalent circuit (Fig. 2). It consists of a source voltage V_s delivering a current I_s , the source reactance is defined by X_s . The considered source is feeding two identical loads Z_A and Z_B passing through a feeder for each load F_A and F_B , each feeder has a reactance x_A and x_B respectively.

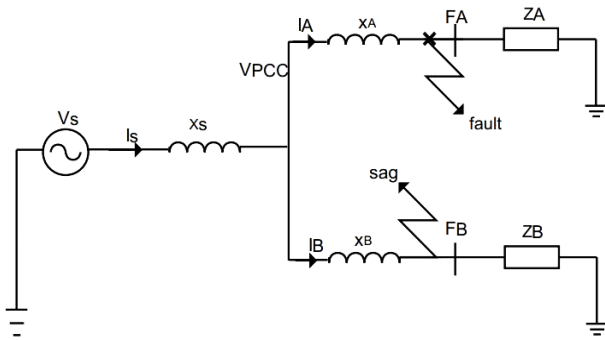


Fig. 2. Equivalent circuit for voltage sag calculation

From the equivalent circuit and basing on Kirchhoff's Law, voltage $V_{pre-sag}$ and current I_s in case of healthy power grid at the point of common coupling are given by:

$$V_{pre-sag} = V_s - I_s X_s ; \quad (1)$$

$$I_s = I_A + I_B = \frac{V_{pre-sag}}{Z_A + x_A} + \frac{V_{pre-sag}}{Z_B + x_B} \quad (2)$$

The current through Z_A and Z_B is the same because of the identical impedances in healthy conditions. At the occurrence fault time on the first feeder, a high circuit current will flow to the broken feeder, on the other side, the current of the second feeder will be reduced. Therefore, the voltage of the second feeder will be decreased as well. This voltage drops is defined as voltage sag. At that point, the source current $I_{s\text{fault}}$ and voltage sag V_{sag} are defined as:

$$V_{sag} = V_s - I_{s\text{fault}} X_s ; \quad (3)$$

$$I_{s\text{fault}} = \frac{V_{sag}}{x_A} + \frac{V_{sag}}{Z_B + x_B} . \quad (4)$$

Thus, DVR must be inserted between the point of common coupling and the sensitive load where the voltage sag takes place. Figure 3 illustrates the DVR placement process.

Most of disturbances in power grid are related to voltage sag and swell. Decreasing and increasing of voltage amplitude at the load side are accompanied by a phase angle jump, for that, control strategies must be adopted to compensate this issue in a very fast way in order to avoid losses of power supply. Figure 4 shows the phasor diagram for a DVR compensation in both voltage sag and voltage swell.

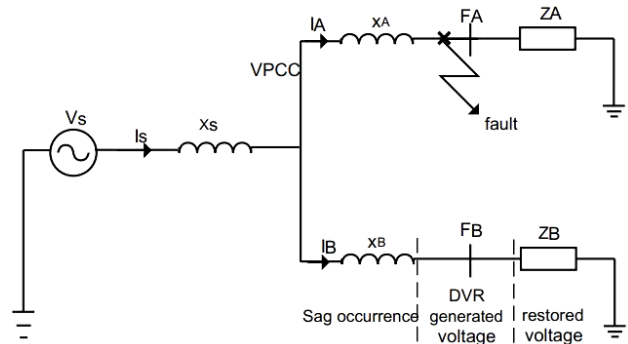


Fig. 3. Equivalent circuit for DVR voltage injection calculation

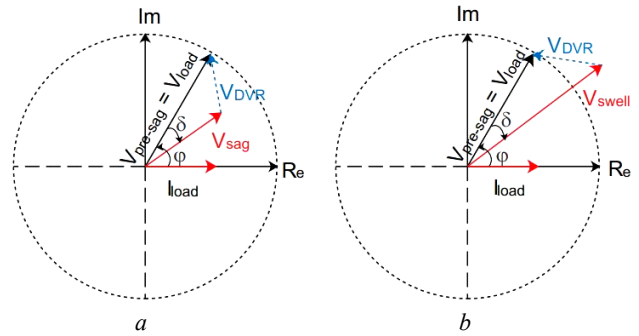


Fig. 4. Phasor diagram for:

(a) voltage sag compensation; (b) voltage swell compensation

3. DVR Control Strategy. The DVR compensates voltage sags by injecting or absorbing reactive power or real power [44]. Reactive power is injected when the DVR voltages are in quadrature with the currents with respect to fundamental frequency, at that point, DVR rely on a self supported dc bus. Nevertheless, active power is injected when the DVR voltages are in phase with the current, thereupon, the need of a battery at the DC bus is necessary.

The voltages references are used to generate the IGBTs gate pulses for the voltage source inverter in a synchronous reference frame. The schematic corresponding to the SRF theory is shown in Fig. 5.

Firstly, source and load voltages are sensed and transformed to a stationary references frame using Concordia transformation as follow:

$$\begin{cases} v_{sa} = \sum_{h=-1}^{+1} V_{sah} \sin(\omega t + \phi_{sah}); \\ v_{sb} = \sum_{h=-1}^{+1} V_{sbh} \sin(\omega t + \phi_{sbh} - \frac{2\pi}{3}); \\ v_{sc} = \sum_{h=-1}^{+1} V_{sch} \sin(\omega t + \phi_{sch} + \frac{2\pi}{3}); \end{cases} \quad (5)$$

$$\begin{cases} v_{La} = \sum_{h=-1}^{+1} V_{Lah} \sin(\omega t + \phi_{Lah}); \\ v_{Lb} = \sum_{h=-1}^{+1} V_{Lbh} \sin(\omega t + \phi_{Lbh} - \frac{2\pi}{3}); \\ v_{Lc} = \sum_{h=-1}^{+1} V_{Lch} \sin(\omega t + \phi_{Lch} + \frac{2\pi}{3}); \end{cases} \quad (6)$$

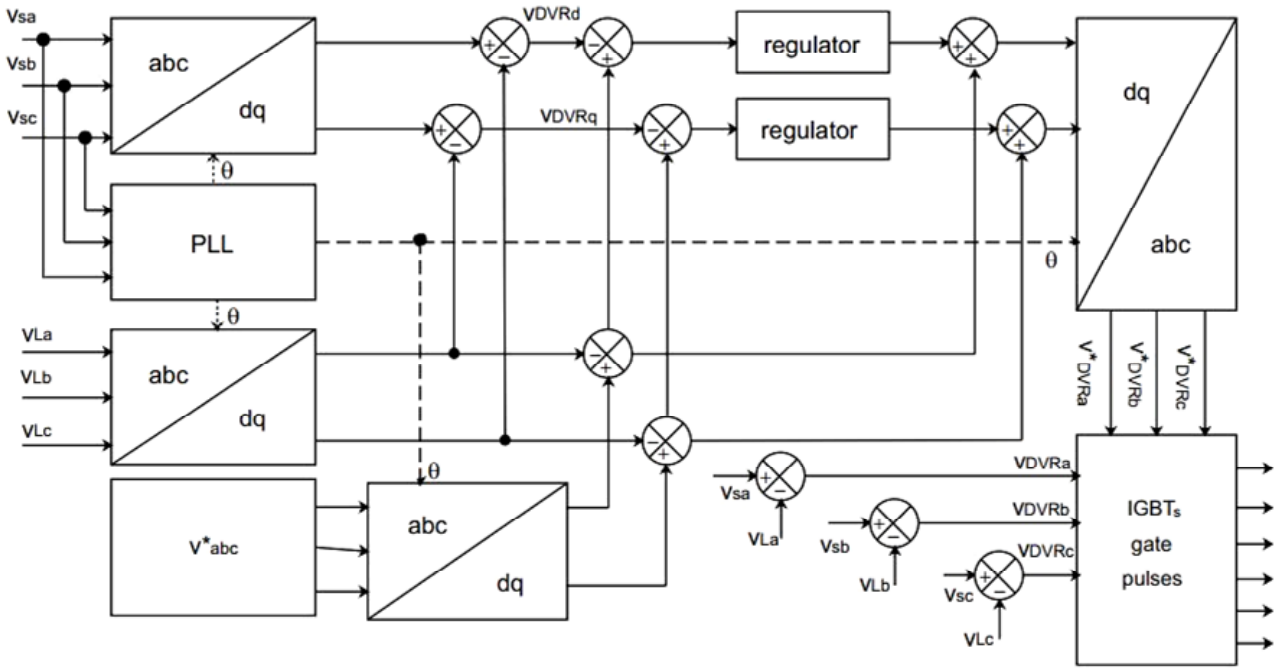


Fig. 5. Block diagram of the SRF control method

where: V_{sa} , V_{sb} and V_{sc} are the voltages source amplitudes; V_{La} , V_{Lb} and V_{Lc} are the voltages load amplitudes; ϕ_{sa} , ϕ_{sb} and ϕ_{sc} are the voltages source phase angles; ϕ_{La} , ϕ_{Lb} and ϕ_{Lc} are the voltages load phase angles; ω is the voltage fundamental pulsation.

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}; \quad (7)$$

$$\begin{bmatrix} v_{L\alpha} \\ v_{L\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix}. \quad (8)$$

Since the voltages are converted to a stationary reference frame, the unit vector derived through a phase locked loop is taking in account to transform these voltages to a synchronous reference frame using Park transformation:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix}; \quad (9)$$

$$\begin{bmatrix} v_{Ld} \\ v_{Lq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} v_{L\alpha} \\ v_{L\beta} \end{bmatrix}. \quad (10)$$

Figure 6 shows the phasor diagram of synchronous transformation. The $\alpha\beta$ coordinates are orthogonal axes obtained from the abc frame. The dq synchronous frame is obtained by rotating the the $\alpha\beta$ coordinates.

The reference load voltages (v_{La}^* , v_{Lb}^* , v_{Lc}^*) are transformed to a synchronous reference frame as well in the same way. In the meantime, the DVR voltage along dq frame could be expressed by:

$$\begin{cases} v_{DVRd} = v_{sd} - v_{Ld}; \\ v_{DVRq} = v_{sq} - v_{Lq}. \end{cases} \quad (11)$$

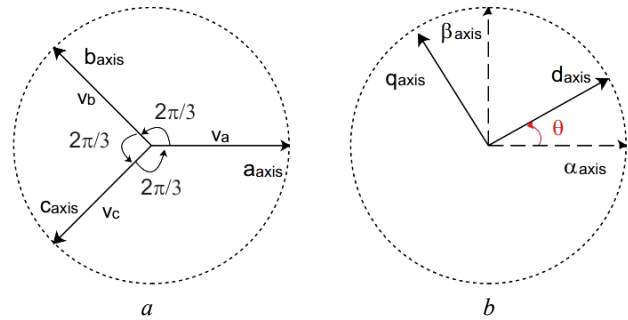


Fig. 6. Phasor diagram exhibits the relation between abc frame (a) and dq frame (b)

Consequently, the DVR reference voltages are obtained by:

$$\begin{cases} v_{DVRd}^* = v_{sd}^* - v_{Ld}; \\ v_{DVRq}^* = v_{sq}^* - v_{Lq}. \end{cases} \quad (12)$$

A controller is used to minimize the error between actual DVR voltages and the generated reference voltage. Lastly, DVR reference voltages are obtained in abc reference frame by applying the Concordia inverse transformation and Park inverse transformation as follow:

$$\begin{bmatrix} v_{DVR\alpha}^* \\ v_{DVR\beta}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} v_{DVRd}^* \\ v_{DVRq}^* \end{bmatrix}; \quad (13)$$

$$\begin{bmatrix} v_{DVRa}^* \\ v_{DVRb}^* \\ v_{DVRc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{DVR\alpha}^* \\ v_{DVR\beta}^* \end{bmatrix}. \quad (14)$$

The three phase voltages system. The balanced three phase voltages system which takes into account any type of distortion can expressed by:

$$\begin{cases} v_{sa} = \sum_{h=-\infty}^{+\infty} V_h \sin(h\omega t + \phi_h); \\ v_{sb} = \sum_{h=-\infty}^{+\infty} V_h \sin(h\omega t + \phi_h - \frac{2\pi}{3}); \\ v_{sc} = \sum_{h=-\infty}^{+\infty} V_h \sin(h\omega t + \phi_h + \frac{2\pi}{3}). \end{cases} \quad (15)$$

The three phase distorted currents form could be represented as follow:

$$\begin{cases} i_{sa} = \sum_{h=-\infty}^{+\infty} I_h \sin(h\omega t + \phi_h); \\ i_{sb} = \sum_{h=-\infty}^{+\infty} I_h \sin(h\omega t + \phi_h - \frac{2\pi}{3}); \\ i_{sc} = \sum_{h=-\infty}^{+\infty} I_h \sin(h\omega t + \phi_h + \frac{2\pi}{3}). \end{cases} \quad (16)$$

where: h denotes the order of the inverse, homopolar and direct harmonic components in the voltage or current systems; V_h , I_h , ϕ_h and ϕ_h are the amplitudes and phase angles of the harmonic components of the voltage and current systems respectively; $\omega = 2\pi f_s$ is the fundamental pulsation of the voltage or current systems.

Phase Locked Loop. Conventional Phase Locked Loop. A PLL principal is based mainly on Park transformation, beyond that, if the instantaneous derivative angle involved in Park transformation is equal to the three phase voltage pulsation system, the components along dq axes will be constant.

The block diagram of a typical PLL is shown in Fig. 7, it contain a phase detector (PD) in order to perform a comparison between the input signal and the arrived one from the Voltage Controlled Oscillator (VCO). Low-pass filter (LPF) is used to correct the error at the PD-output.

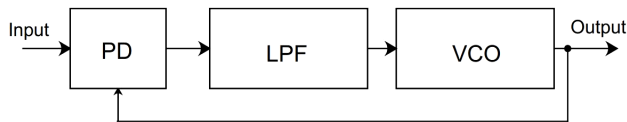


Fig. 7. Typical phase locked loop block diagram

The PLL consider the utility voltages expressed by Eq. (5), then, it goes to a synchronous frame passing by stationary frame using Eq. (7) and Eq. (9). After all calculation, the obtained equation is given by:

$$\begin{cases} v_d = V_s \sin(\theta - \theta_{mes}); \\ v_q = V_s \cos(\theta - \theta_{mes}). \end{cases} \quad (17)$$

From Eq. (17) one can notice that, if the phase angle error $\theta_z = \theta - \theta_{mes}$ is small, than this equation becomes:

$$v_d = V_s (\theta - \theta_{mes}). \quad (18)$$

At the moment $\theta = \theta_{mes}$, the PLL is locked, on the other hand, if $\theta \neq \theta_{mes}$, the phase error is governed by a controller adjusting ω until $\theta = \theta_{mes}$.

To accomplish the above explained phase lock, we consider the following block diagram of the locked loop as shown in Fig. 8.

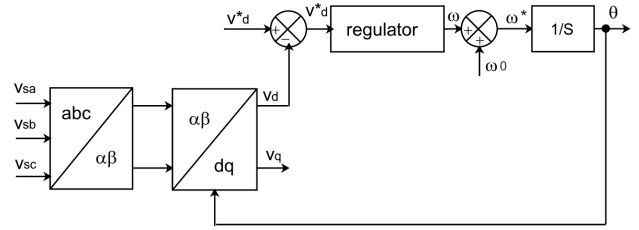


Fig. 8. Three phase PLL structure diagram

Proposed-Phase Locked Loop. The main purpose of any PLL configuration is to generate a unite vector containing the utility phase angle in order to pass to a synchronous reference frame. The proposed configuration is based on a Multi Variable Filter (MVF) to generate a \sin and \cos unite vectors directly that contain the utility phase angle information.

The transfer function of the MVF is based on 'Hong-Seok-Song' work. Its formulation is expressed by the following equation

$$\begin{cases} \tilde{x}_\alpha(s) = \frac{k(s+k)}{(s+k)^2 + \omega_c^2} x_\alpha(s) - \frac{k\omega_c}{(s+k)^2 + \omega_c^2} x_\beta(s); \\ \tilde{x}_\beta(s) = \frac{k(s+k)}{(s+k)^2 + \omega_c^2} x_\beta(s) + \frac{k\omega_c}{(s+k)^2 + \omega_c^2} x_\alpha(s), \end{cases} \quad (19)$$

where x_α , x_β are the input signals and \tilde{x}_α , \tilde{x}_β are the fundamental output signals.

From its formulation, the MVF filter is similar to a band-pass filter in the output response. Conversely, the integral effect of the MVF is neglected because it does not introduce a phase shift to the output signal regarding to its input. By way of explanation, both input and outputs MVF's signals have the same phase angle.

The developed analytical formulation of Eq. (19), could be given by:

$$\begin{cases} \tilde{x}_\alpha = \sqrt{\frac{3}{2}} \sum_{h=-\infty}^{+\infty} \frac{I_h}{\sqrt{1 + \left(\frac{(1-h)\omega}{k}\right)^2}} \begin{pmatrix} \sin\left(h\omega t + \phi_h + a \tan\left(\frac{(1-h)\omega}{k}\right)\right) \\ -e^{-kt} \sin\left(h\omega t + \phi_h + a \tan\left(\frac{(1-h)\omega}{k}\right)\right) \end{pmatrix} \\ \tilde{x}_\beta = -\sqrt{\frac{3}{2}} \sum_{h=-\infty}^{+\infty} \frac{I_h}{\sqrt{1 + \left(\frac{(1-h)\omega}{k}\right)^2}} \begin{pmatrix} \cos\left(h\omega t + \phi_h + a \tan\left(\frac{(1-h)\omega}{k}\right)\right) \\ -e^{-kt} \cos\left(h\omega t + \phi_h + a \tan\left(\frac{(1-h)\omega}{k}\right)\right) \end{pmatrix} \end{cases} \quad (20)$$

Eq. (20) shows that the MVF effectiveness in cancelation any kind of disturbance is related principally to the constant k . Indeed, it is obvious if k is taken small, the disturbances will be attenuated perfectly. Otherwise, the transient time response will increase in parallel which is explained by the exponential part. In this case, taking k so small, Eq. (20) takes the following form:

$$\begin{cases} \tilde{x}_\alpha = \sqrt{\frac{3}{2}} (1 - e^{-kt}) \sin(\omega t + \phi_1); \\ \tilde{x}_\beta = -\sqrt{\frac{3}{2}} (1 - e^{-kt}) \cos(\omega t + \phi_1). \end{cases} \quad (21)$$

The concept is to hold back the voltage disturbance as possible in order to get a correct phase angle information which lead to a correct DVR control. A unit vector is obtained instantaneously without any phase

shift by taking k so small, the negative aspect of large time response is defeated. The unit vector is defined by Eq. (22):

$$\begin{cases} \frac{\tilde{x}_\alpha(t)}{\sqrt{\tilde{x}_\alpha^2 + \tilde{x}_\beta^2}} = \sin(\omega t + \varphi_1); \\ \frac{\tilde{x}_\beta(t)}{\sqrt{\tilde{x}_\alpha^2 + \tilde{x}_\beta^2}} = \cos(\omega t + \varphi_1). \end{cases} \quad (22)$$

4. Performances of the proposed PLL. To examine the proposed PLL performances, several tests have been accomplished. In the first case, a balanced three phase source voltages are considered as presented in Fig. 9.

From Fig. 9,a.1 and Fig. 9,b.1 one can notice that, the classical and proposed PLL have similar behavior where they produce suitable unit vectors, it is obvious from the presented phase angles as shown in Fig. 9,a.2 and Fig. 9,b.2.

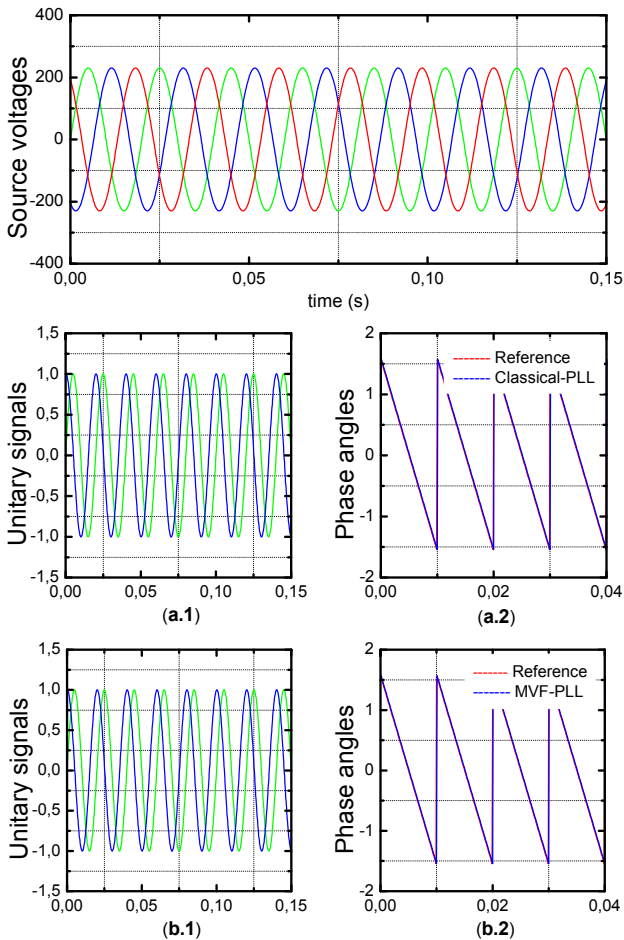


Fig. 9. Simulation results, Case 1: Balanced source voltages

The second case of study takes unbalanced three phase voltages without harmonics expressed in a total mitigation of voltage phase as shown in Fig. 10.

In this case, the classical PLL fails in extracting the sin and cosine signals from the unbalanced source voltages as presented in Fig. 10,a.1, this fact leads to a phase angle shifting from its reference as illustrated in Fig. 10,a.2.

On the other hand, the proposed PLL still give pure unit vectors in Fig. 10,b.1, with a soft phase angle shifting

from $t = 0$ s to $t = 0.01$ s, which is totally acceptable under these sever unbalance conditions as shown in Fig. 10,b.2.

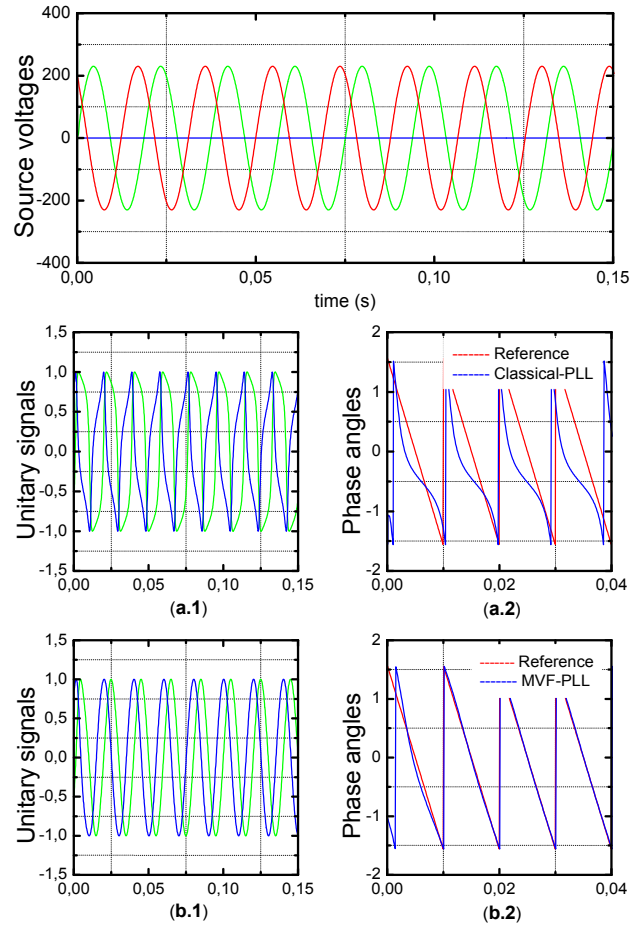


Fig. 10. Simulation results, Case 2: Unbalanced source voltages

The three phase source voltages are considered balanced and distorted by injecting the third and the fifth harmonics in the main voltages defined by the following equations:

$$\begin{cases} v_a = V_{a1} \sin(\omega t + \varphi_{a1}) + V_{a3} \sin(3\omega t + \varphi_{a3}) + \\ + V_{a5} \sin(5\omega t + \varphi_{a5}); \\ v_b = V_{b1} \sin\left(\omega t + \varphi_{b1} - \frac{2\pi}{3}\right) + V_{b3} \sin\left(3\omega t + \varphi_{b3} - \frac{2\pi}{3}\right) + \\ + V_{b5} \sin\left(5\omega t + \varphi_{b5} - \frac{2\pi}{3}\right); \\ v_c = V_{c1} \sin\left(\omega t + \varphi_{c1} + \frac{2\pi}{3}\right) + V_{c3} \sin\left(3\omega t + \varphi_{c3} + \frac{2\pi}{3}\right) + \\ + V_{c5} \sin\left(5\omega t + \varphi_{c5} + \frac{2\pi}{3}\right). \end{cases} \quad (23)$$

Figure 11 describes the three phase distorted voltages. From Fig. 11,a.1 and Fig. 11,a.2 it is clear that the classical PLL exhibits poor capacities in extracting the unit vectors containing the phase angle information. Otherwise, the proposed PLL still present high capability in giving an instantaneous unit vector even the presence of harmonics in the three phase source voltages as illustrated in Fig. 11,b.1 and Fig. 11,b.2.

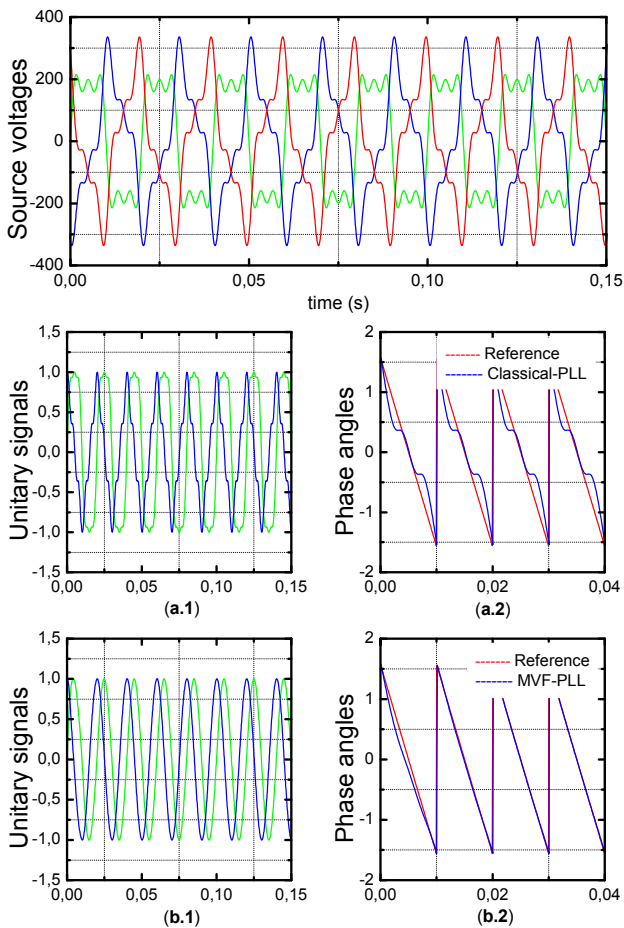


Fig. 11. Simulation results, Case 3: Balanced distorted source voltages

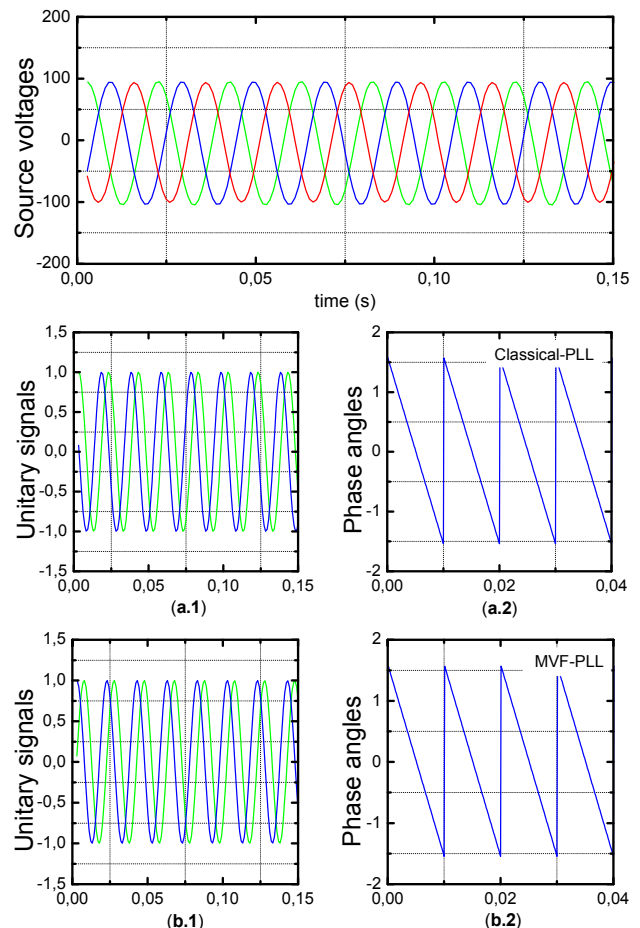


Fig. 13. Experimental results, Case 1: Balanced source voltages

Experimental validation. The proposed method performances are verified through simulation and experiment validations using Dspace 1104 platform as shown in Fig 12. Hardware parameters and control parameters used in experimental test are summarized in Table 1.



Fig. 12. Experimental platform

Table 1

Experimental parameters				
V_s	V_{dc}	C_{dc}	I_f	K_{MVF}
110 V	300 V	1100 μ F	4 mH	0.0001

Figure 13 presents the balanced three phase voltages. In this case both classical PLL and the proposed one success in extracting unitary signals that contains the phase angle information as shown in Figs. 13,a.1, a.2 and Figs. 13,b.1, b.2.

Figure 14 shows unbalanced three phase voltages expressed in taking-off the second phase. One can notice that, the classical PLL fails in extracting unitary signals as shown in Fig. 14,a.1 which leads to certain loss of phase angle information as presented in Fig. 14,a.2. On the other hand, the proposed MVF-PLL is motionless to this kind of unbalance and gives acceptable unit vectors and phase angle quality as shown in Fig. 14,b.1 and Fig. 14,b.2.

The last test is based on generating harmonics on the three phase source voltage as it generated in the simulation section. It is clear from Fig. 15 that the source voltages contain a huge amount of harmonics which weaken the classical PLL in extracting fundamental phase angle as shown in Fig. 15,a.1 and Fig. 15,a.2. Where, the MVF-PLL preserves its capability in giving true information in experiment tests as in simulation.

The aim of the second section of experimental study is dedicated to examine the dynamic voltage restorer under various conditions. Indeed, the first case is expressed in introducing a voltage sag in one phase by inserting a resistor in that phase in order to have the desired sag from $t = 8:27$ s to $t = 8:44$ s as it is shown in Fig. 16,a.1. The reference component required to compensate that sag is presented in Fig. 16,a.2. It is clear that, the DVR hits in rejecting the introduced voltage sag perfectly as it is illustrated in Fig. 16,a.3.

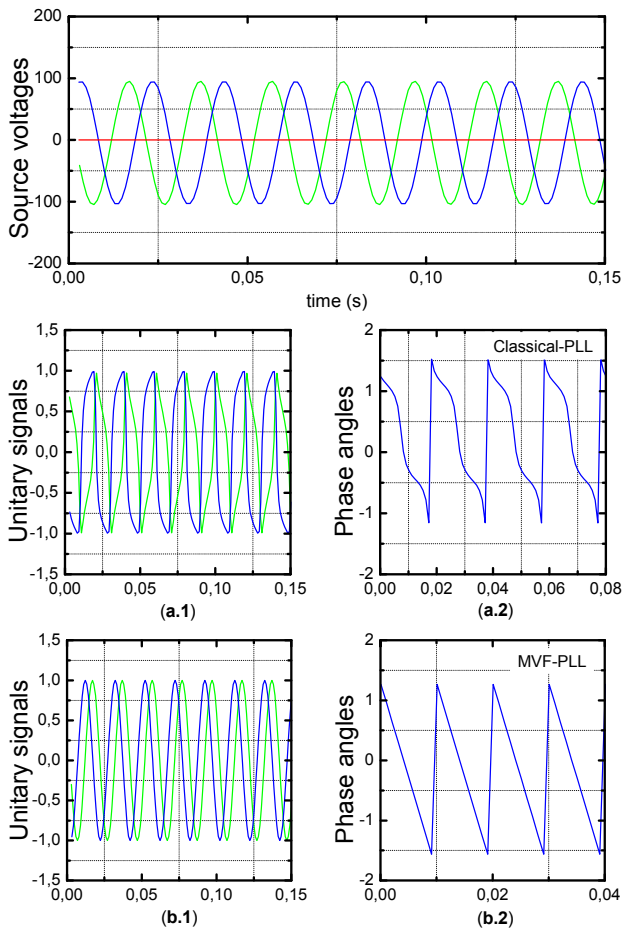


Fig. 14. Experimental results, Case 2: Unbalanced source voltages

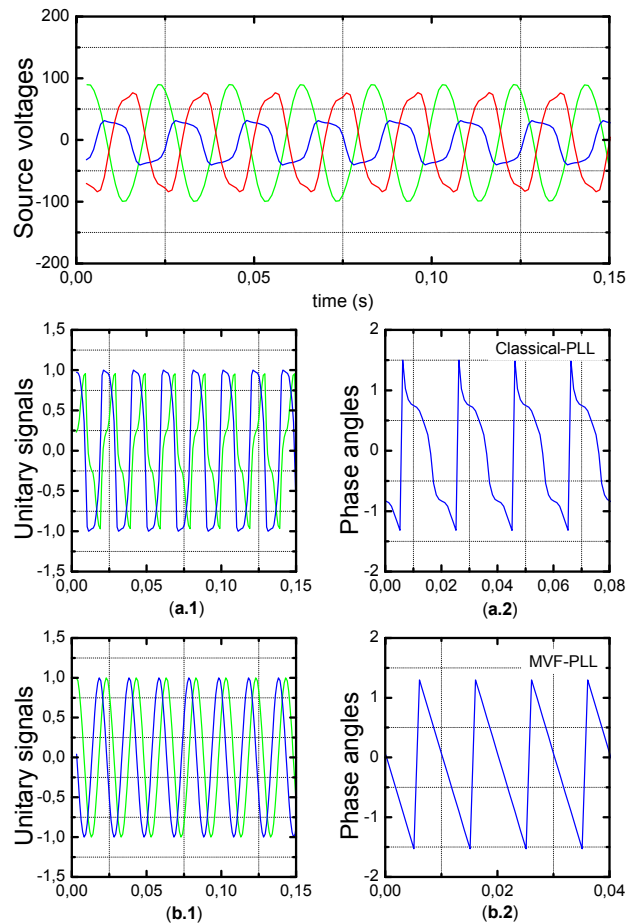


Fig. 15. Experimental results, Case 3: Balanced distorted source voltages

Fig. 16,b.1 presents a voltage sags of two phases in three phase source voltages from $t = 1:65$ s to $t = 2:15$ s. This case is considered as one of the most spread sags in the grid networks. From Fig. 16,b.2, one can notice that, the enhanced algorithm gives coherent reference voltages to compensate that occurred on the grid and make it balanced sinusoidal as shown in Fig. 16,b.3.

To put the dynamic voltage restorer under more sever conditions a three phase voltage sag is considered from $t = 2:54$ s to $t = 2:67$ s in the third test as shown in Fig. 16,c.1. The DVR still generate the wanted voltages as shown in Fig. 16,c.2, to compensate the occurred sag on the grid and ensure the balanced three phase voltages of the grid, Fig. 16,c.3.

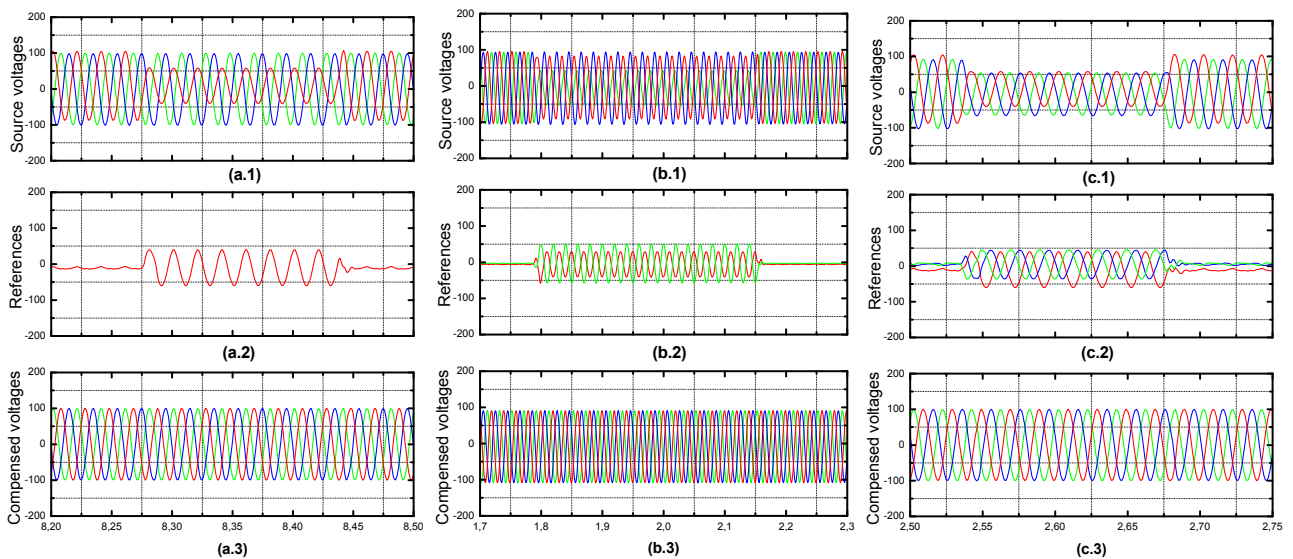


Fig. 16. Experimental results, DVR behavior under different conditions

Conclusions.

Voltage sag is a crucial problem for industries, indeed, it introduces malfunction for customer's equipments. Researchers have investigated numerous solutions to mitigate the harmful effect of voltage sag. Dynamic voltage restorer is one of the most famous solutions. In this paper, authors have introduced an enhanced algorithm based on synchronous reference frame to control a dynamic voltage restorer for voltage sags rejection. The presented algorithm is based on a Multi variable filter in order to synthesize unitary signals containing fundamental phase angle information involved in generating necessary voltages for compensating the occurred sags. The considered algorithm is tested under different conditions such as single phase sag, two phase sag and three phase sag, on the other hand, the Multi variable filter configuration is examined under the most severe conditions such as a total phase exclusion and in the case of a huge amount of harmonic presence, where elimination of harmonics is not our case of study in this paper but to show the effectiveness of the proposed algorithm in synthesizing the unitary signals. The efficiency of the introduced method is validated by simulation and experimental results.

Conflict of interest. The authors declare that they have no conflicts of interest.

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